22883

PATENT TRADEMARK OFFICE

PATENT

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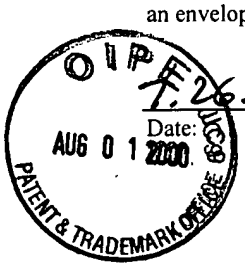

F.26.00 Arlette Malhas

Date: By: Arlette Malhas

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Regula, J.		
Assignee:	Sebring Systems.		
Title:	Method and Apparatus for a Fault Tolerant, Software Transparent and High Data Integrity Extension to a Backplane Bus or Interconnect		
Serial No.:	09/421,771	Filed:	10/19/99
Examiner:	Not Yet Assigned.	Group Art Unit:	2737

Attorney Docket No.: 136.1001.04

Los Altos, California
Date: July 26, 2000

BOX ISSUE FEE (Amendments)
c/o Technology Center 2700
US PATENT AND TRADEMARK OFFICE
Washington, D.C. 20231

SUBMISSION OF PROPOSED DRAWING AMENDMENT FOR APPROVAL BY EXAMINER (37 CFR 1.121(a)(3)(ii))

Sir:

Attached please find a copy of the original of Fig.s 2, 5b, 13a, 13b, and 21 with red ink markings, showing the proposed changes to the drawing in this application. Applicant requests the Examiner to approve the proposed changes.

The proposed change to Fig. 21 corrects a mislabeled signal line 2115.

The proposed change to Fig. 5b moves the signal lines on Fig. 5b to new Fig. 5c to respond to the draftsperson's objection as to view and enlarged view. The proposed change to Fig. 2 is also responsive to this objection.

On reviewing the drawings, we determined that Fig. 13a, and 13b had similar view problems and added brackets accordingly.

No new matter was added by these proposed changes.

We are ready to file the formal drawings and await your approval prior to doing so.

If I can be of any additional assistance, please do not hesitate to contact me at (650) 947-0700 x309.

Respectfully submitted,

Dated: 7-26-00

John C. Merchant
Attorney for Applicants
Reg. No.: 45,996

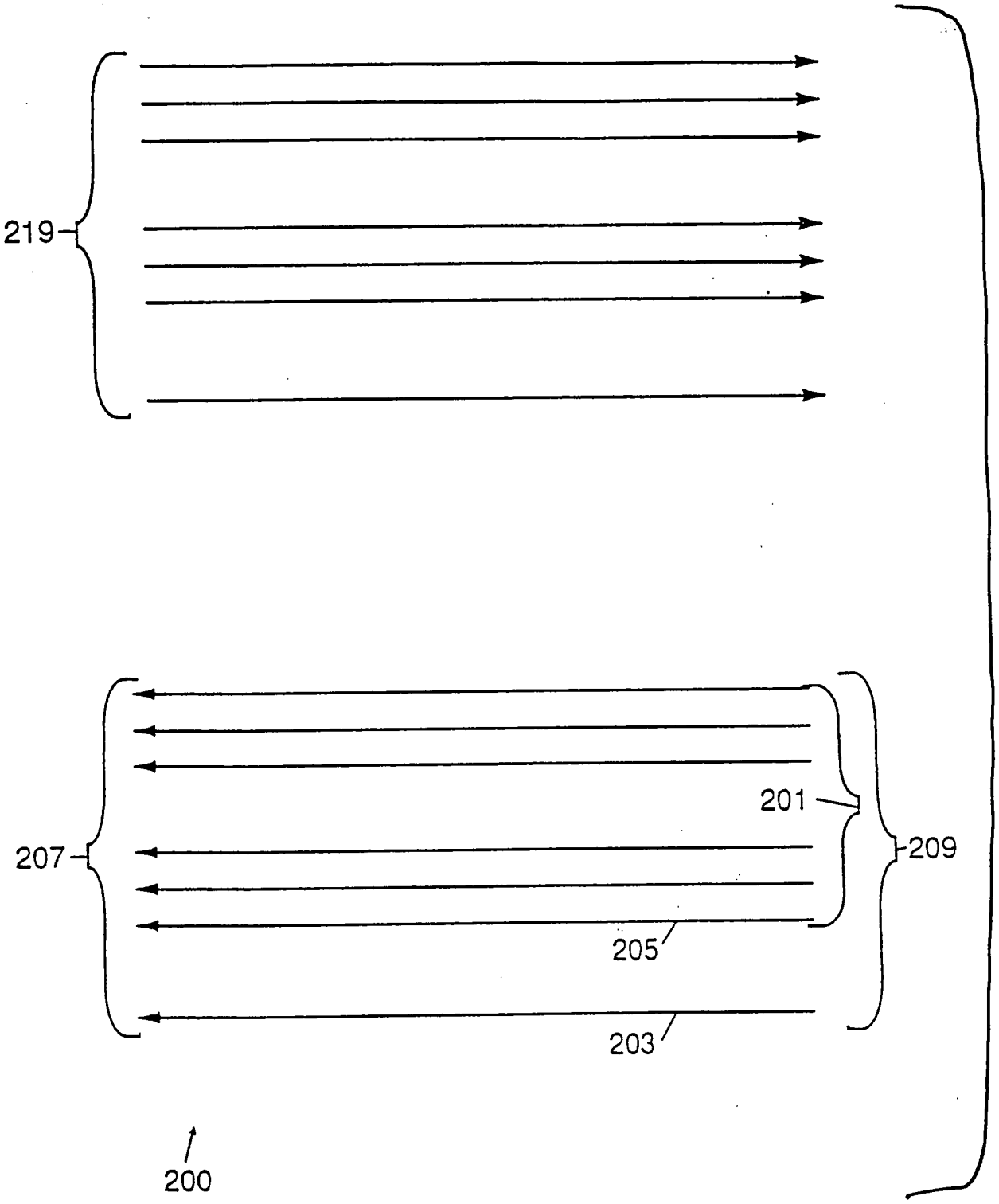

Fig. 2

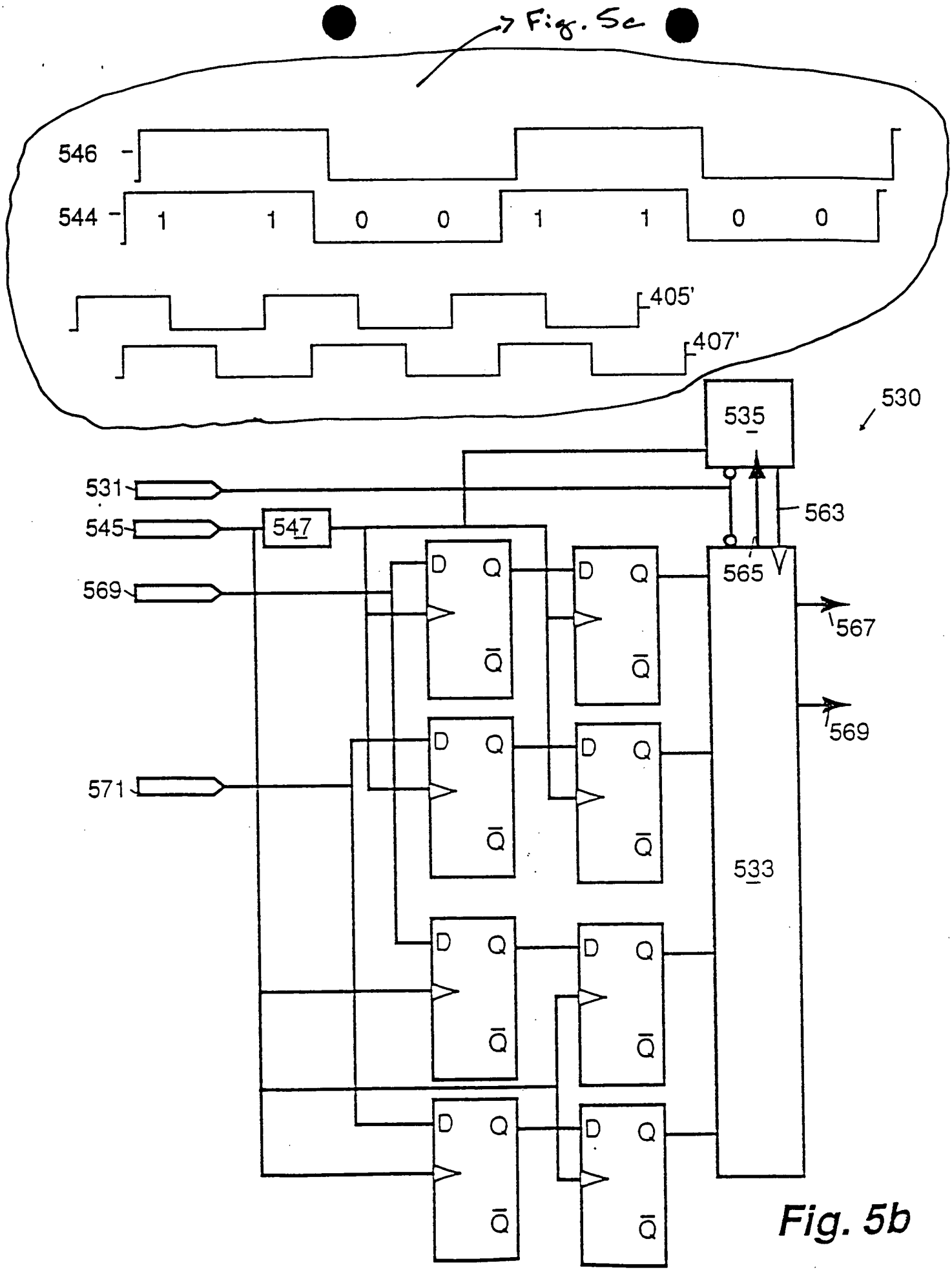
Fig. 5c
546
544
1
1
0
0
1
1
0
0
405'
407'
530
535
531
545
547
563
569
565
567
569
571
533
D
Q
$\bar{Q}$

Fig. 5b

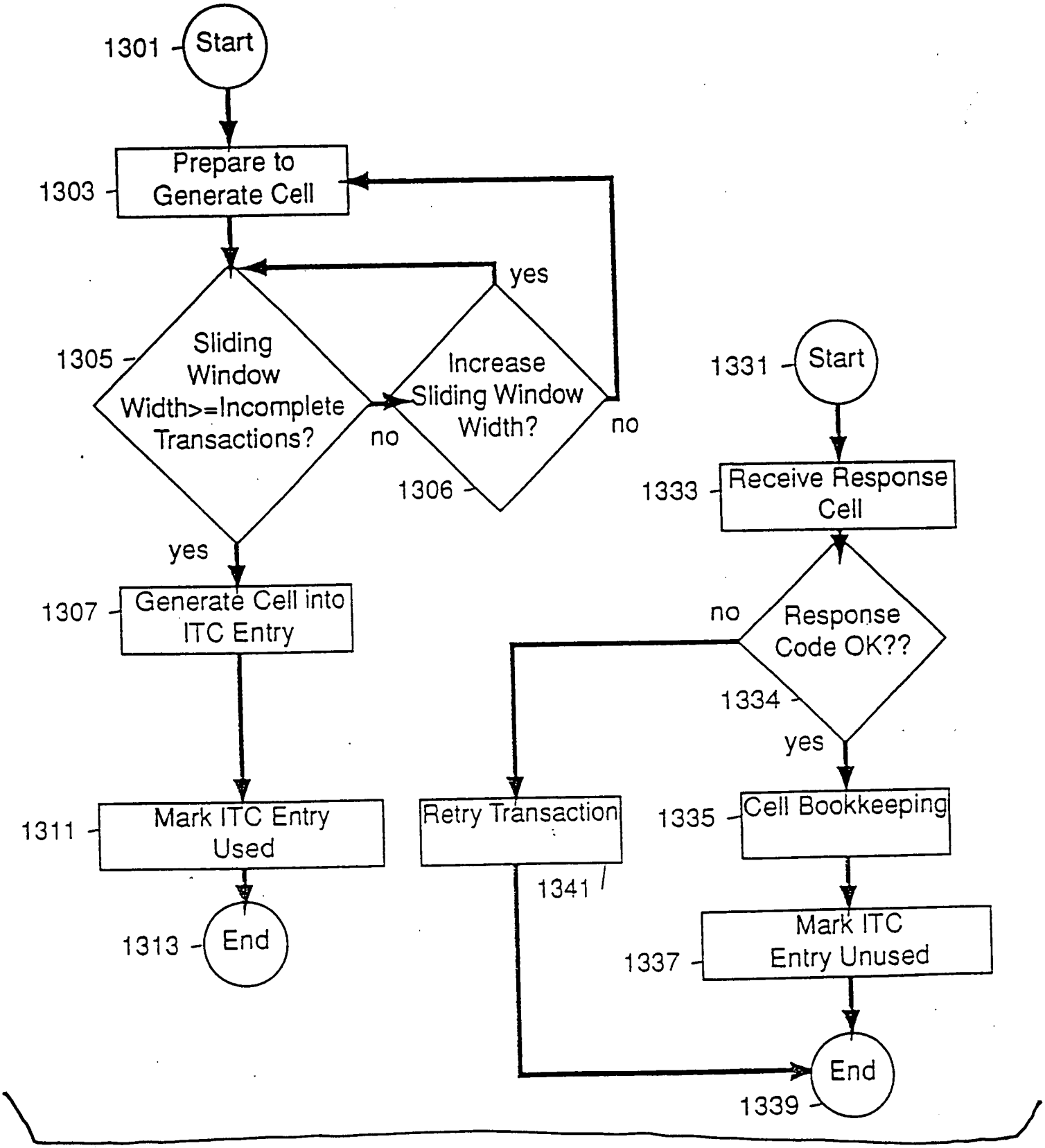
1301
Start
1303
Prepare to Generate Cell
1305
Sliding Window Width>=Incomplete Transactions?
yes
no
1306
Increase Sliding Window Width?
yes
no
1307
Generate Cell into ITC Entry
1311
Mark ITC Entry Used
1313
End
1331
Start
1333
Receive Response Cell
1334
Response Code OK??
no
yes
Retry Transaction
1341
1335
Cell Bookkeeping
1337
Mark ITC Entry Unused
End
1339

Fig. 13a

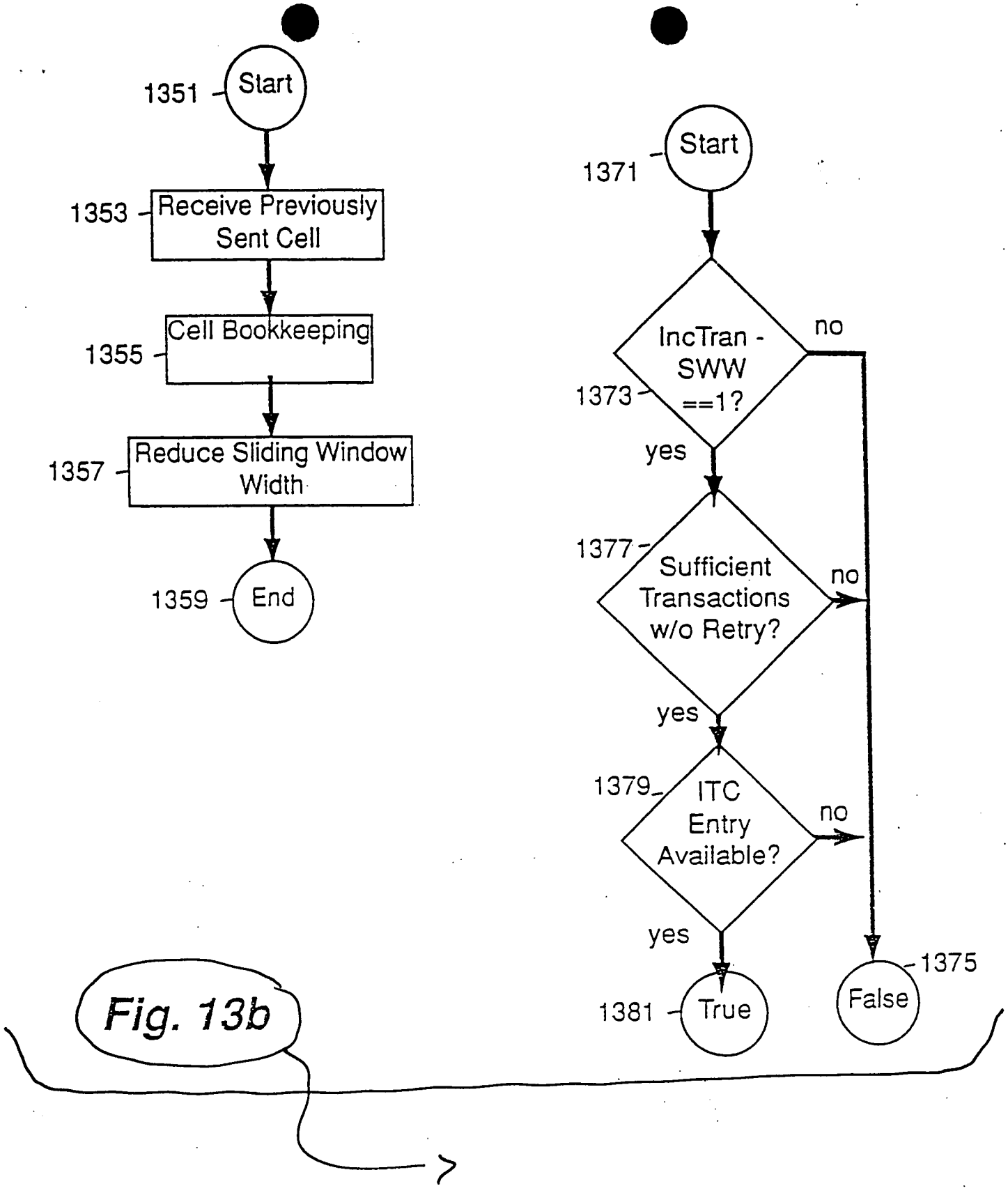
1351
Start
1353
Receive Previously Sent Cell
1355
Cell Bookkeeping
1357
Reduce Sliding Window Width
1359
End
1371
Start
IncTran - SWW ==1?
1373
no
yes
1377
Sufficient Transactions w/o Retry?
no
yes
1379
ITC Entry Available?
no
yes
1381
True
False
1375

Fig. 13b

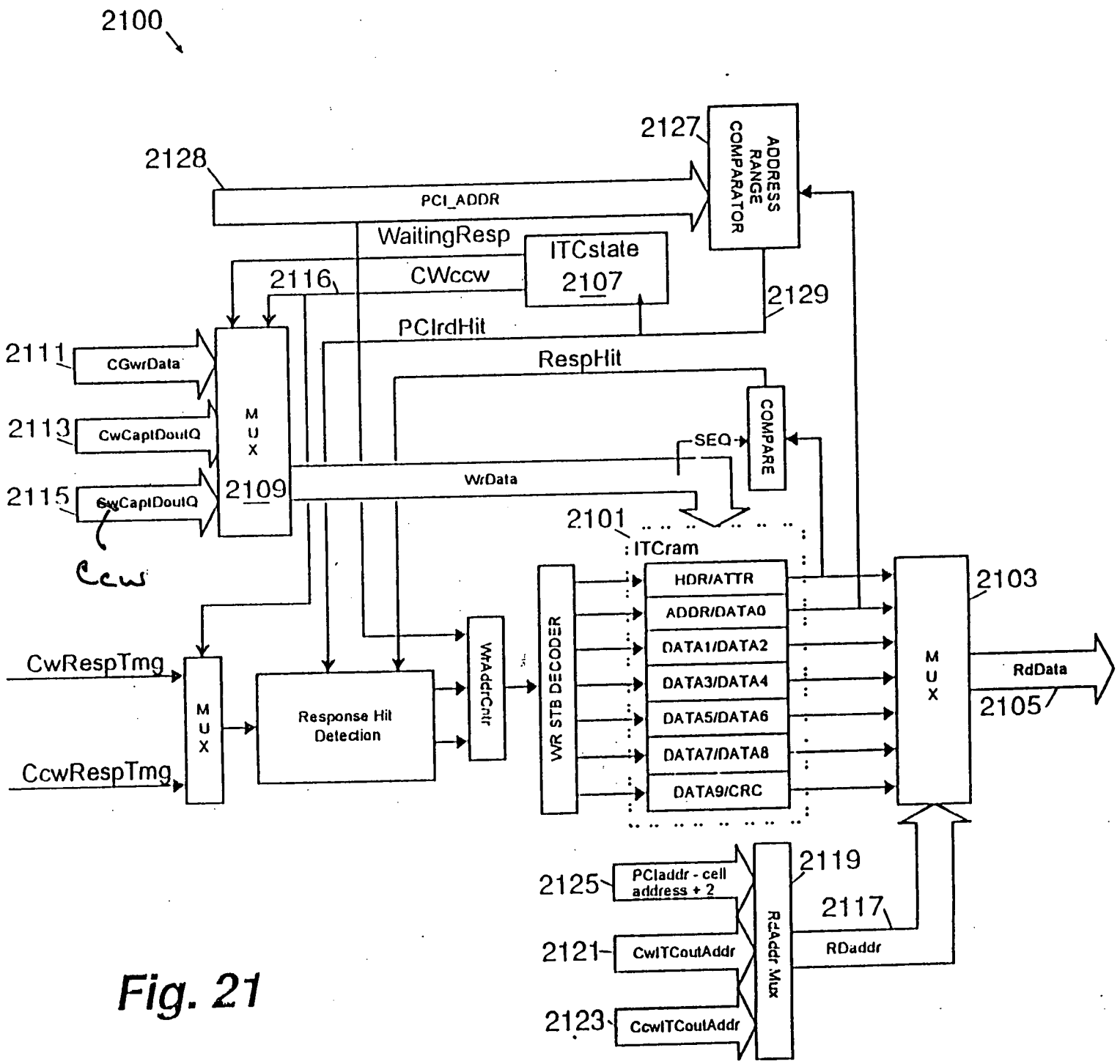
2100
2127
ADDRESS RANGE COMPARATOR
2128
PCI_ADDR
WaitingResp
ITCstate
2107
2116
CWccw
2129
PCIrdHit
RespHit
2111
CGwrData
2113
CwCaptDoutQ
2115
CcwCaptDoutQ
MUX
2109
SEQ
COMPARE
WrData
2101
ITCram
HDR/ATTR
ADDR/DATA0
DATA1/DATA2
DATA3/DATA4
DATA5/DATA6
DATA7/DATA8
DATA9/CRC
WR STB DECODER
WrAddrCntr
2103
RdData
2105
CwRespTmg
CcwRespTmg
Response Hit Detection
2125
PCIaddr - cell address + 2
2119
2117
2121
CwITCoutAddr
RDaddr
2123
CcwITCoutAddr
RdAddr Mux

Fig. 21

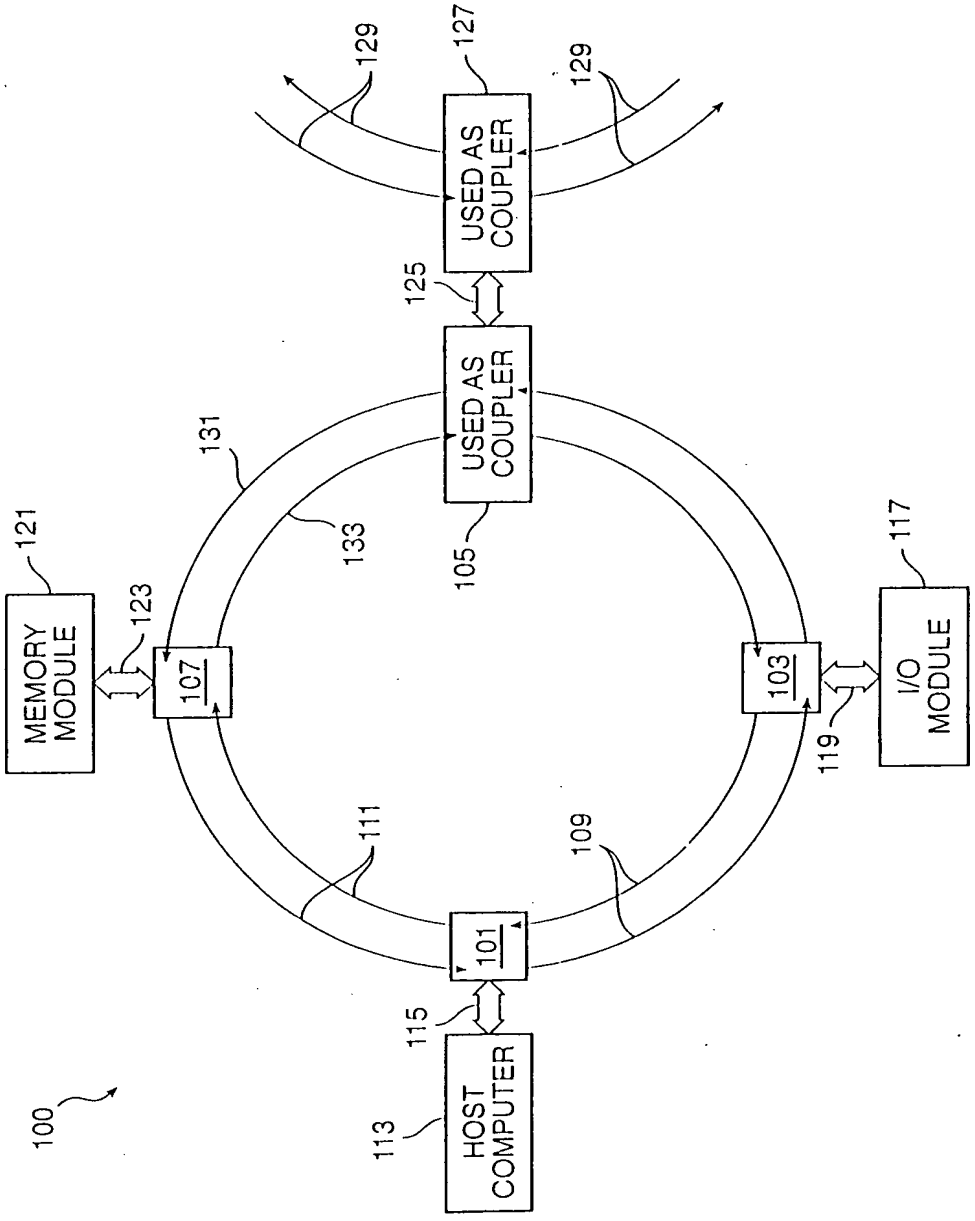
100
HOST COMPUTER
113
115
101
111
109
107
123
MEMORY MODULE
121
131
133
USED AS COUPLER
105
125
USED AS COUPLER
127
129
129
103
119
I/O MODULE
117

FIG. 1a

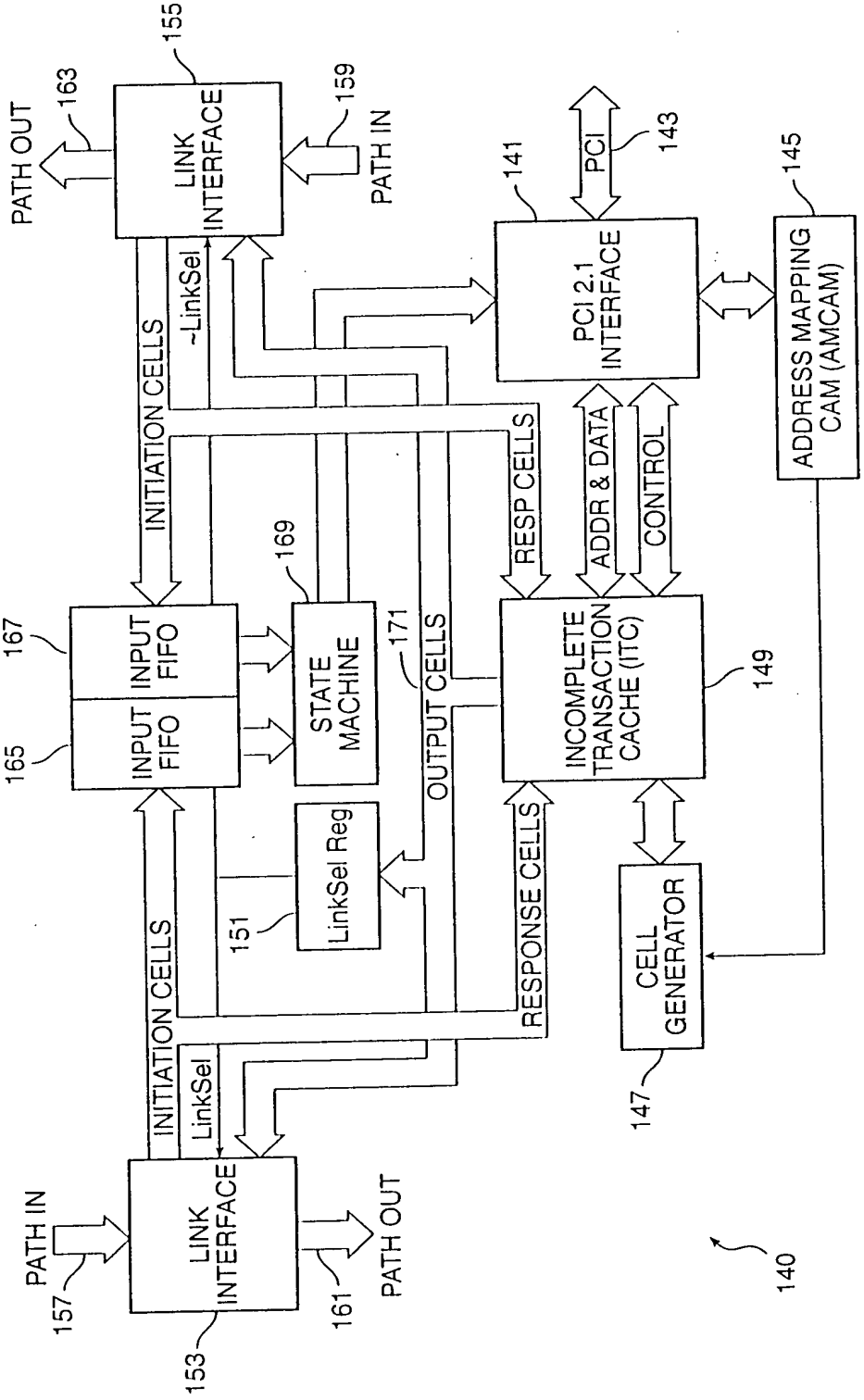
PATH OUT
163
155
LINK INTERFACE
159
PATH IN
141
PCI
143
145
PCI 2.1 INTERFACE
ADDRESS MAPPING CAM (AMCAM)
~LinkSel
INITIATION CELLS
RESP CELLS
ADDR & DATA
CONTROL
169
167
INPUT FIFO
INPUT FIFO
165
STATE MACHINE
171
OUTPUT CELLS
INCOMPLETE TRANSACTION CACHE (ITC)
149
LinkSel Reg
151
RESPONSE CELLS
CELL GENERATOR
147
INITIATION CELLS
LinkSel
PATH IN
157
LINK INTERFACE
161
PATH OUT
153
140

FIG. 1b

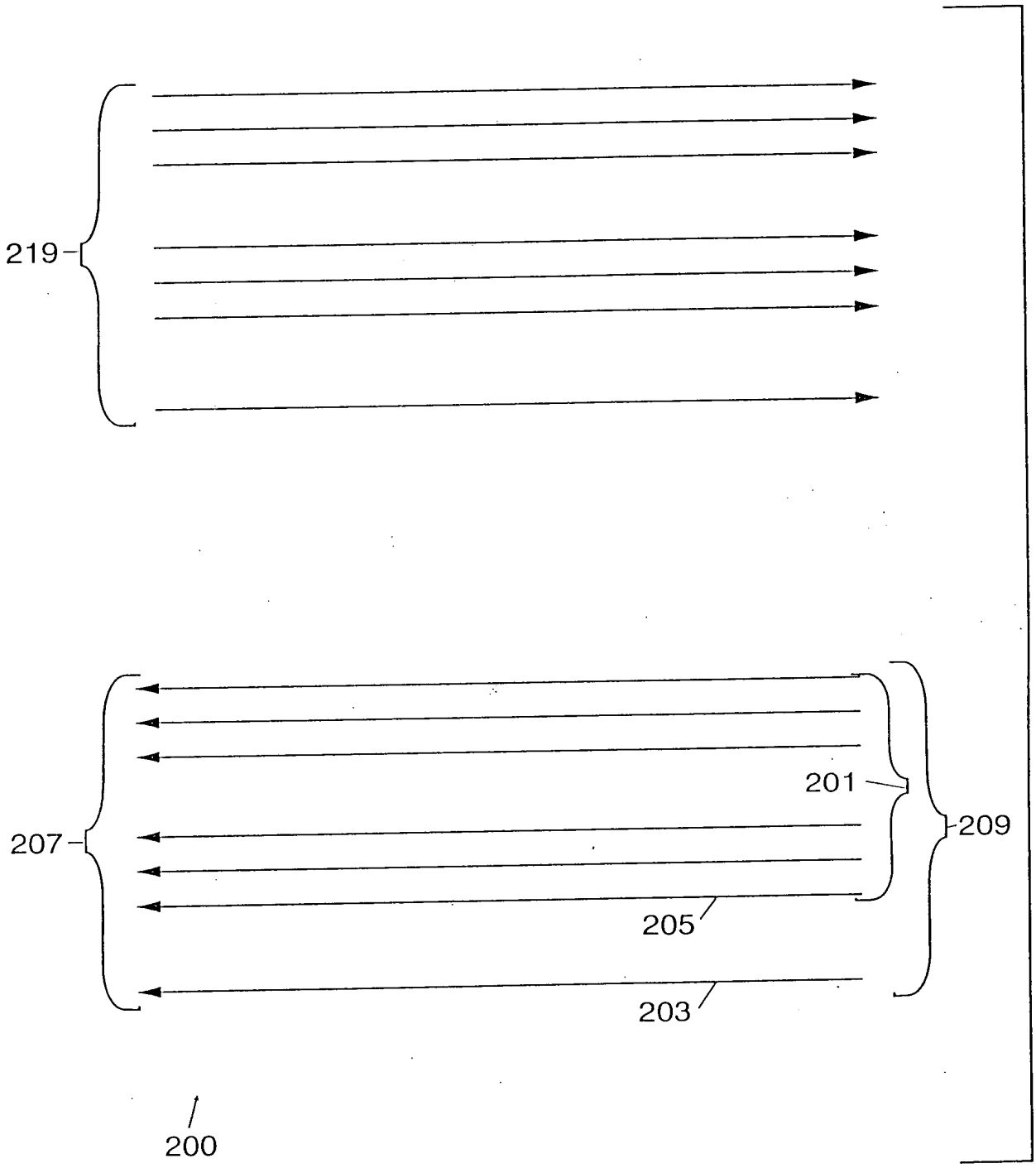

Fig. 2

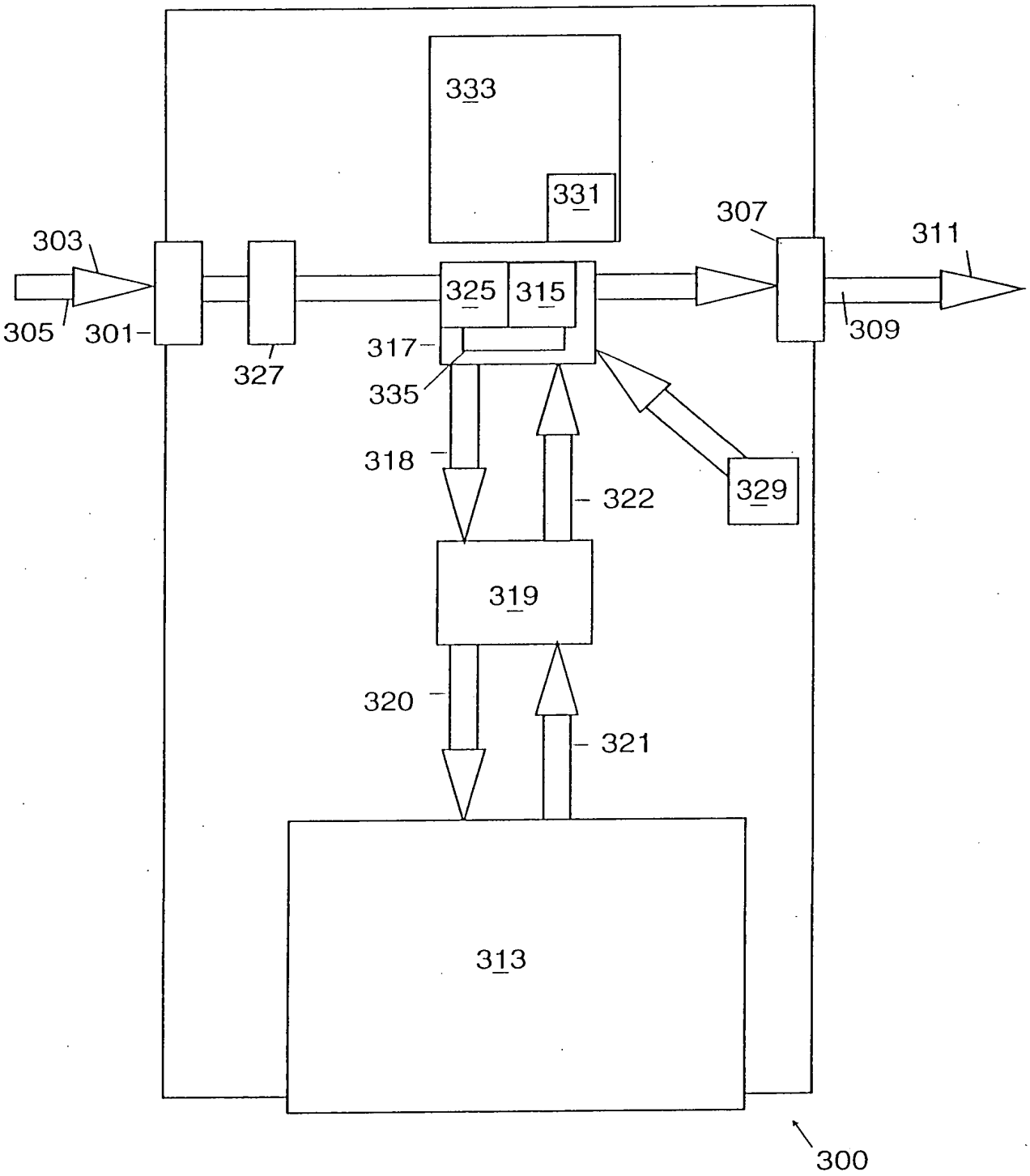
333
331
303
305
301
327
325
315
317
335
307
311
309
318
322
329
319
320
321
313
300

Fig. 3

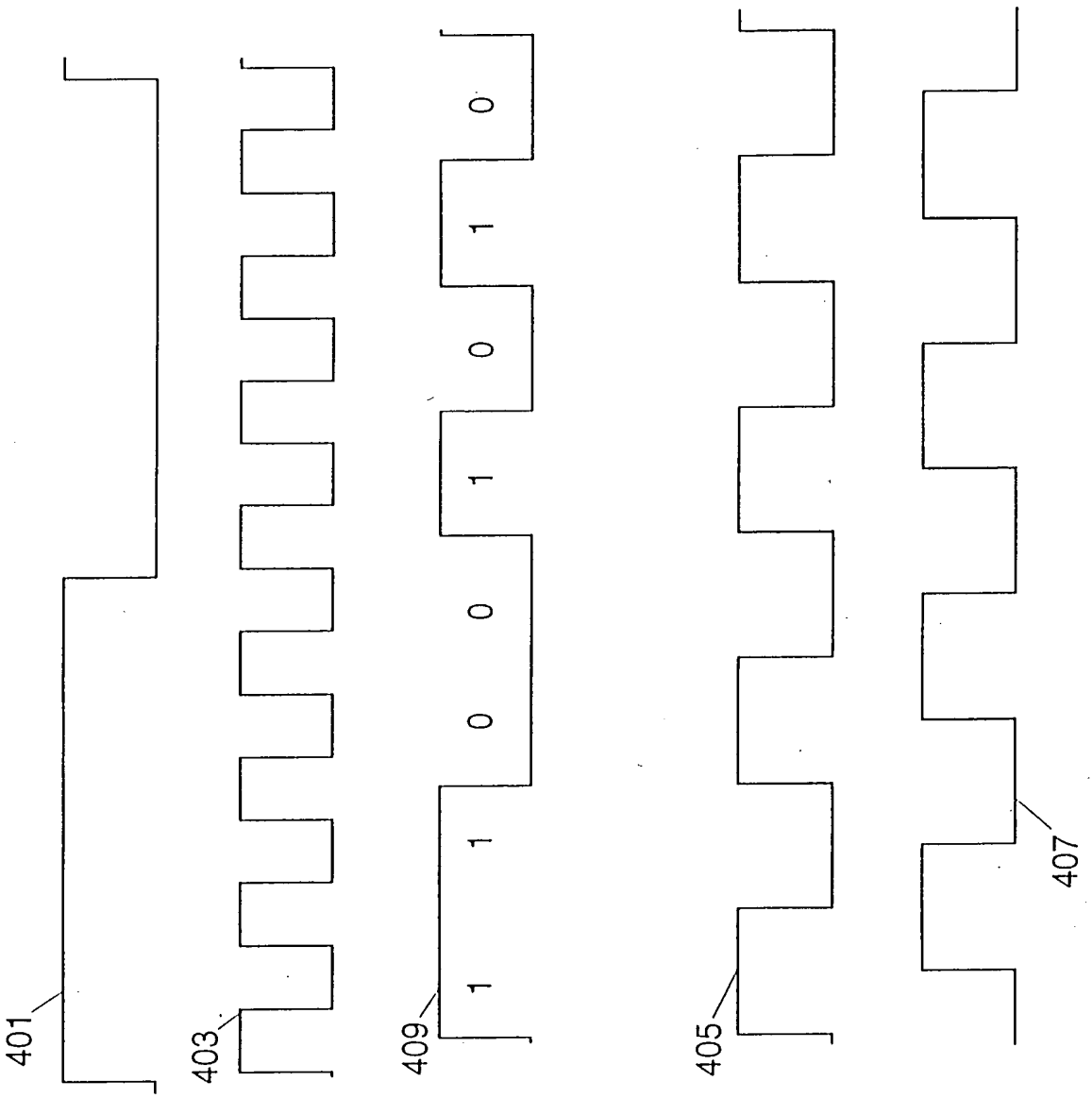

Fig. 4

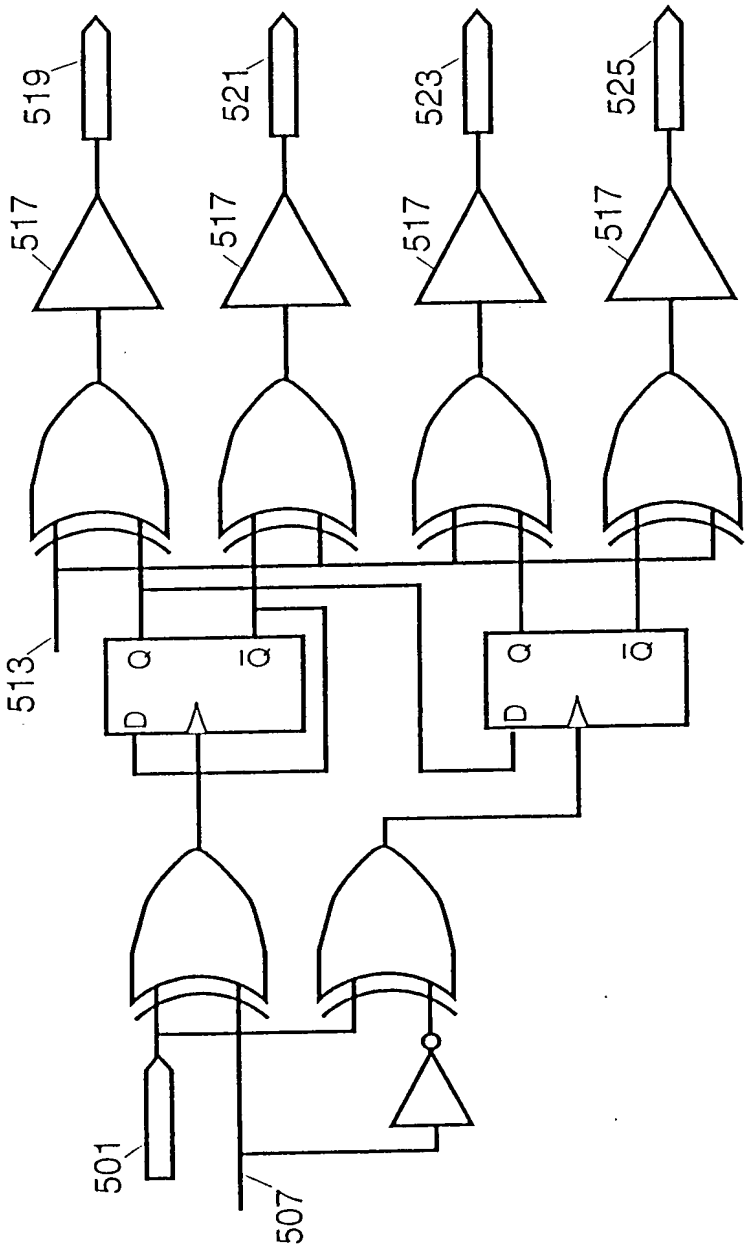

Fig. 5a

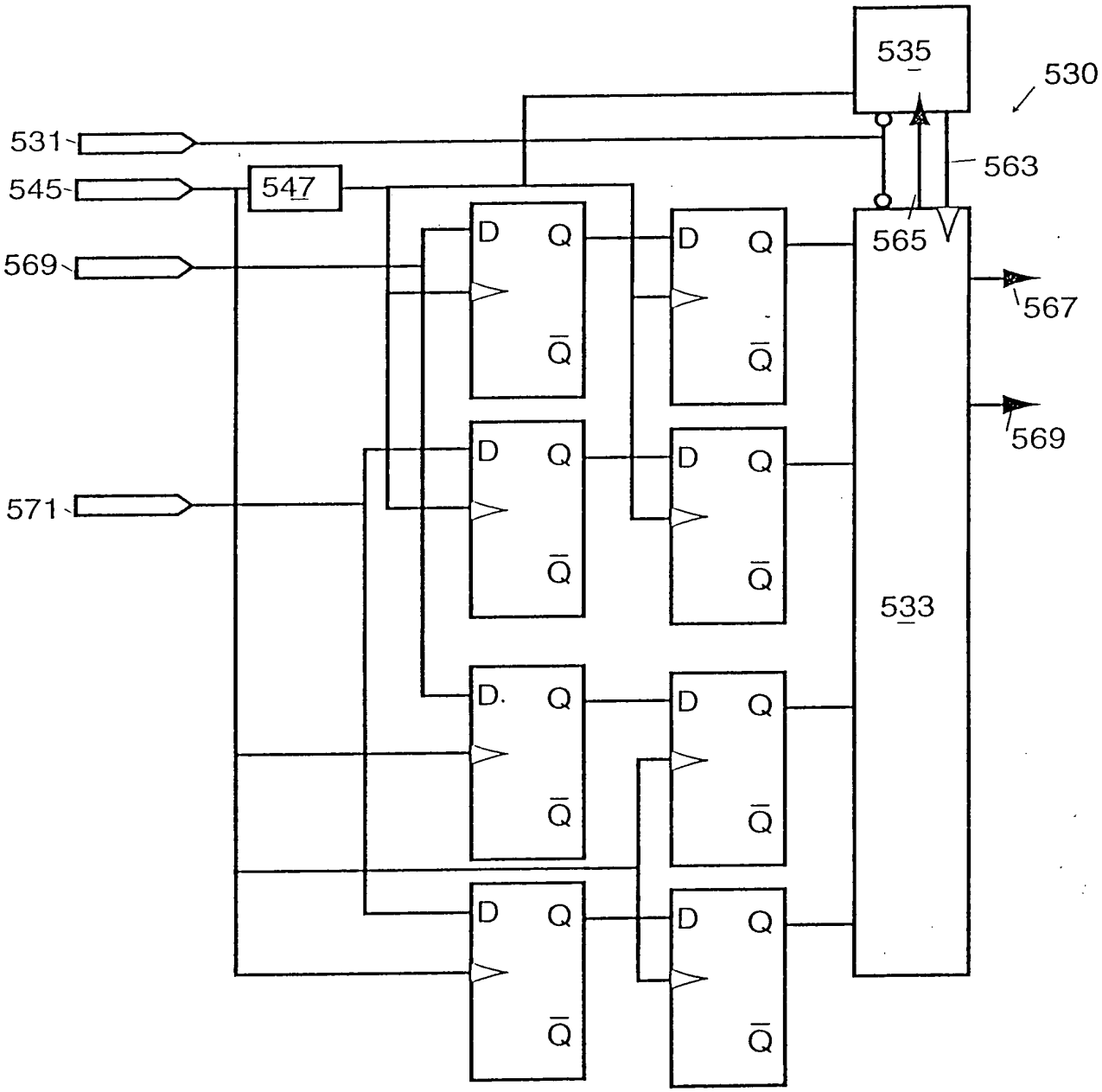

Fig. 5b

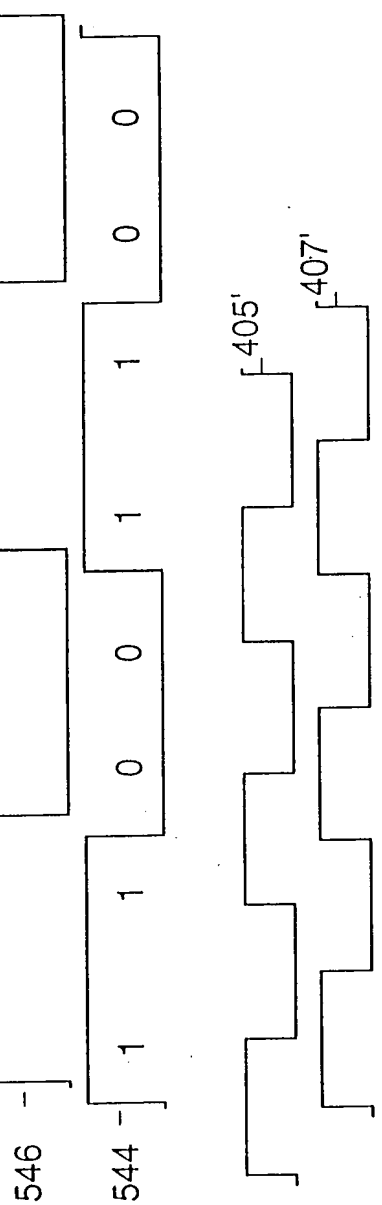

Fig. 5c

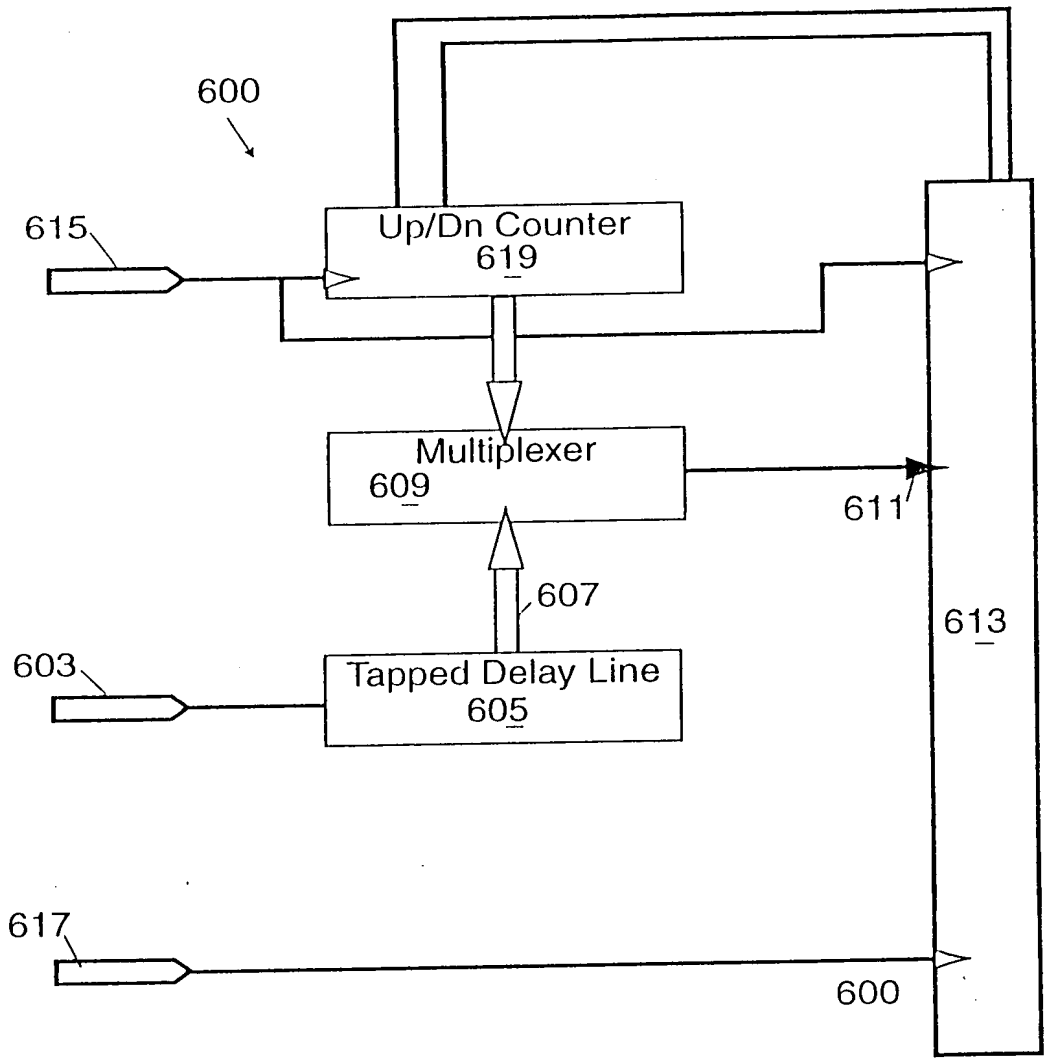
600
615
Up/Dn Counter
619
Multiplexer
609
611
607
613
603
Tapped Delay Line
605
617
600

Fig. 6

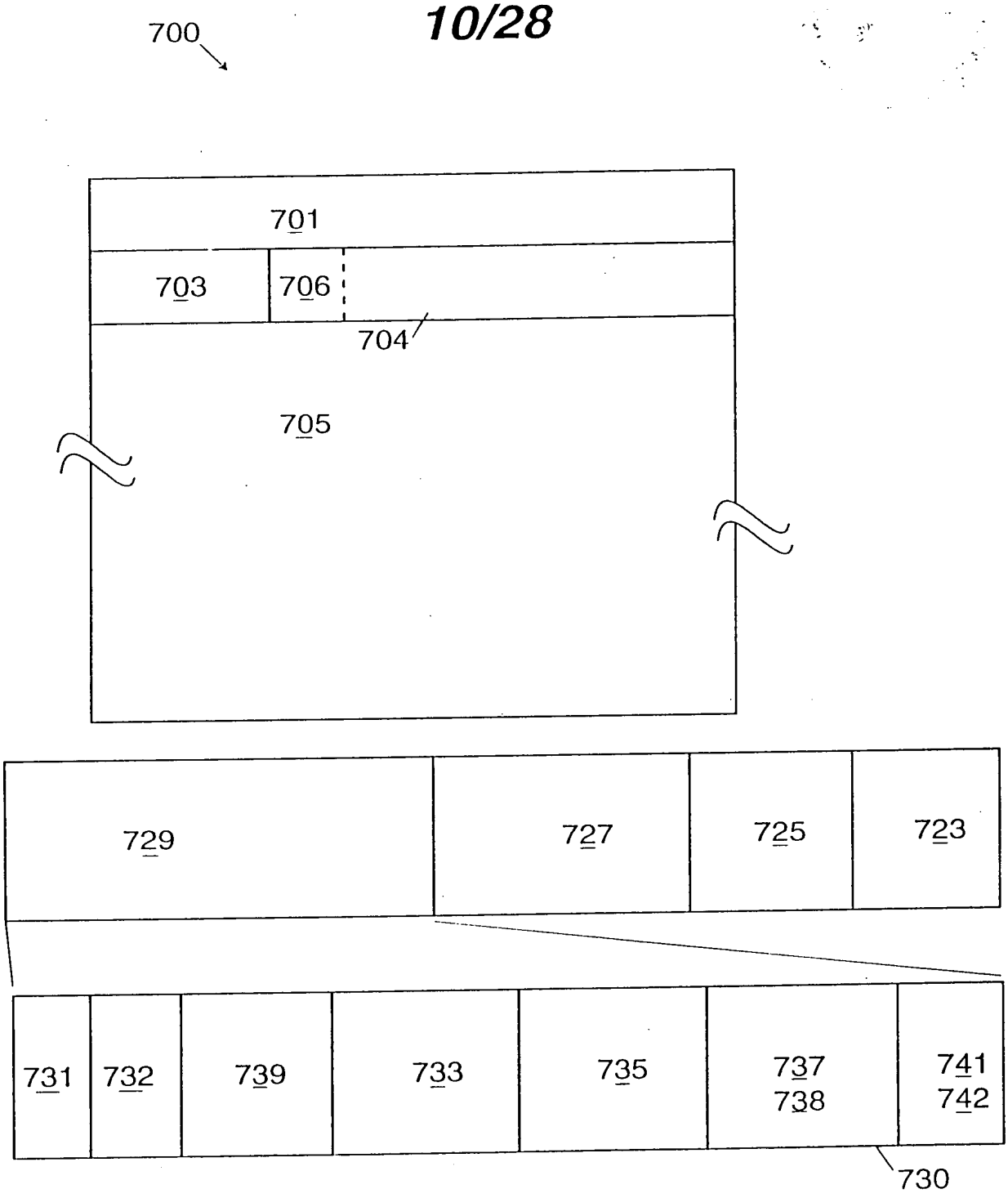
700
701
703
706
704
705
729
727
725
723
731
732
739
733
735
737
738
741
742
730

Fig. 7

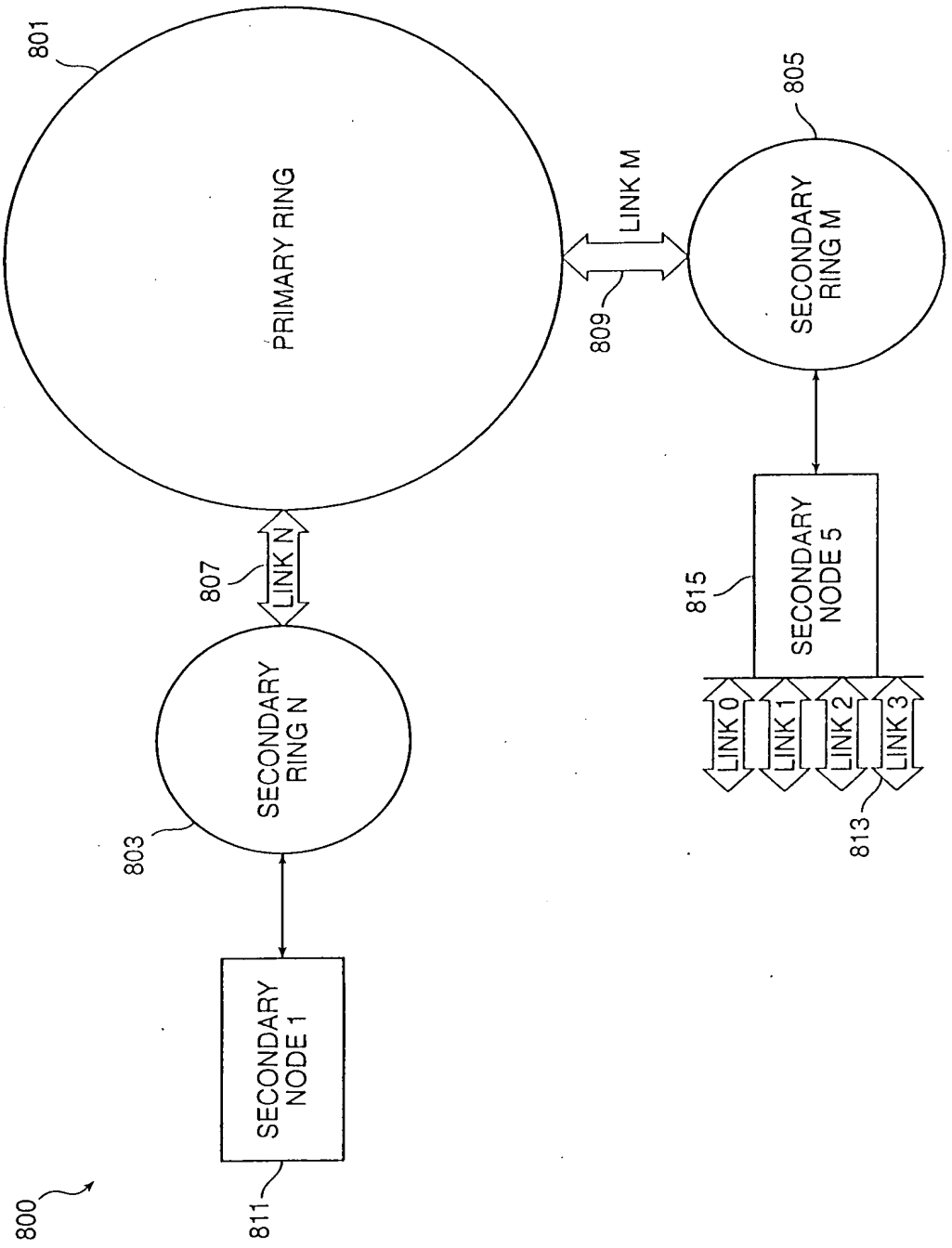
800
801
PRIMARY RING
803
SECONDARY RING N
805
SECONDARY RING M
807
LINK N
809
LINK M
811
SECONDARY NODE 1
813
LINK 0
LINK 1
LINK 2
LINK 3
815
SECONDARY NODE 5

FIG. 8

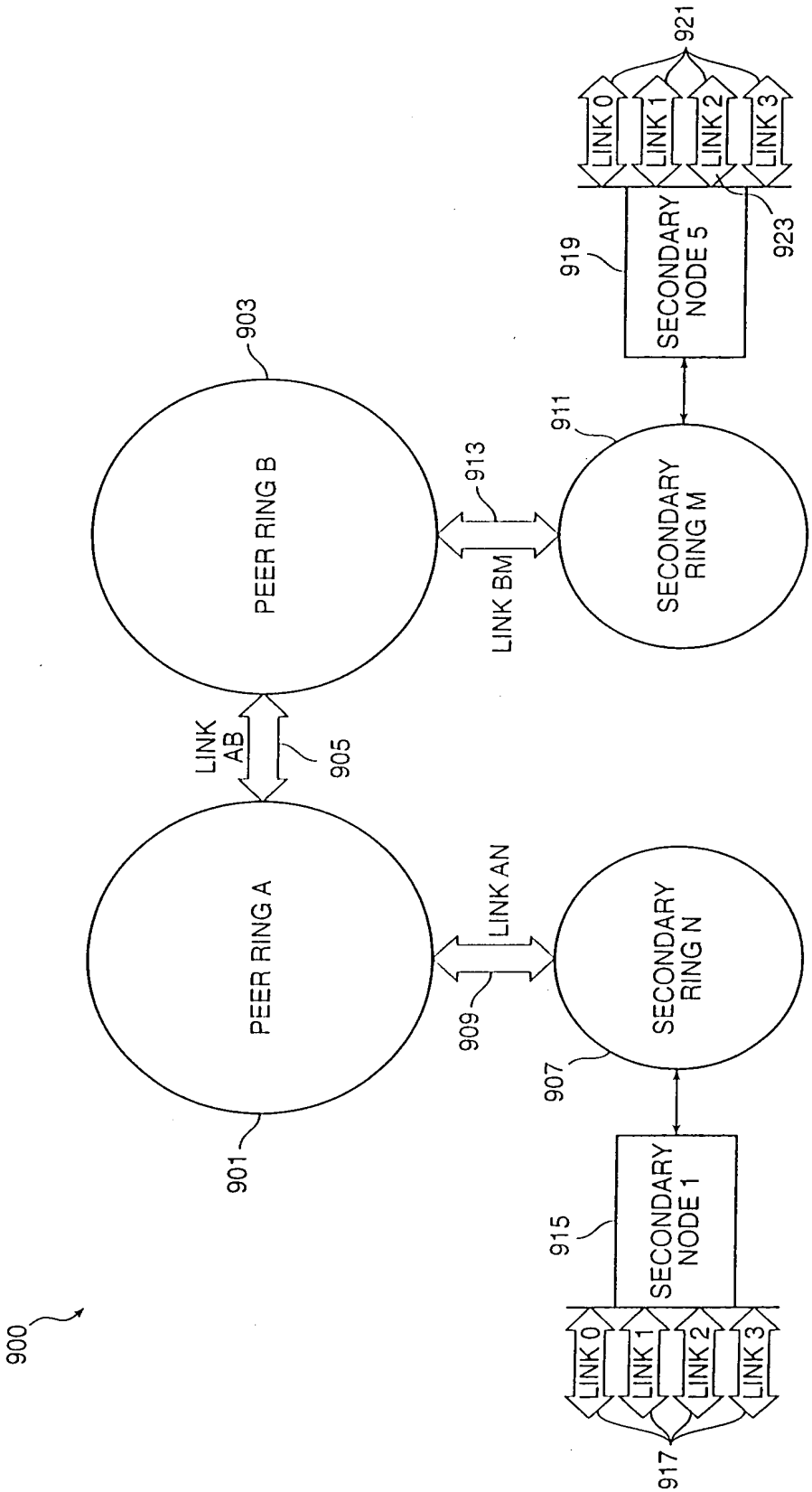
900
PEER RING A
PEER RING B
SECONDARY RING N
SECONDARY RING M
SECONDARY NODE 1
SECONDARY NODE 5
LINK AB
LINK AN
LINK BM
LINK 0
LINK 1
LINK 2
LINK 3
901
903
905
907
909
911
913
915
917
919
921
923

FIG. 9

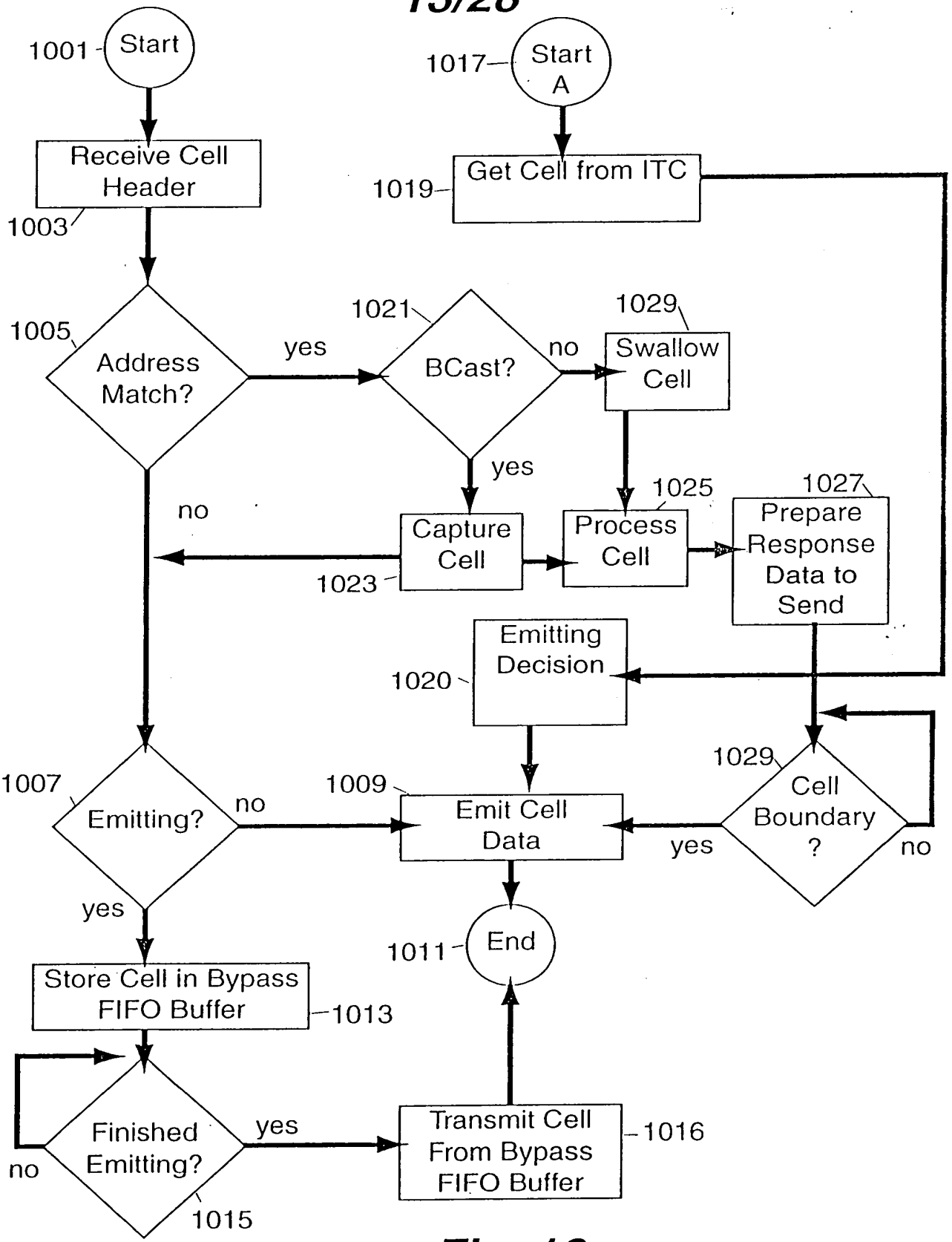
1001
Start
Receive Cell Header
1003
1005
Address Match?
yes
1021
BCast?
no
1029
Swallow Cell
yes
no
Capture Cell
1023
1025
Process Cell
1027
Prepare Response Data to Send
1017
Start A
1019
Get Cell from ITC
1020
Emitting Decision
1007
Emitting?
no
1009
Emit Cell Data
1029
Cell Boundary ?
yes
no
yes
1011
End
Store Cell in Bypass FIFO Buffer
1013
Finished Emitting?
yes
no
1015
Transmit Cell From Bypass FIFO Buffer
1016

Fig. 10

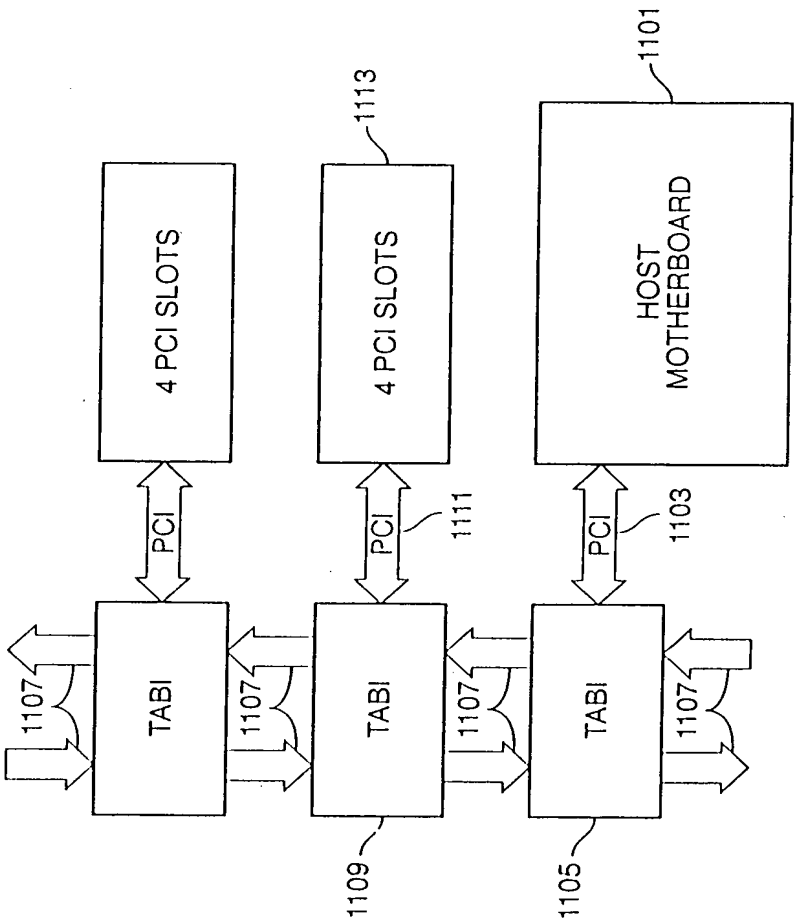
1101
HOST MOTHERBOARD
1113
4 PCI SLOTS
4 PCI SLOTS
PCI
PCI
PCI
1111
1103
TABI
TABI
TABI
1107
1107
1107
1107
1109
1105

FIG. 11

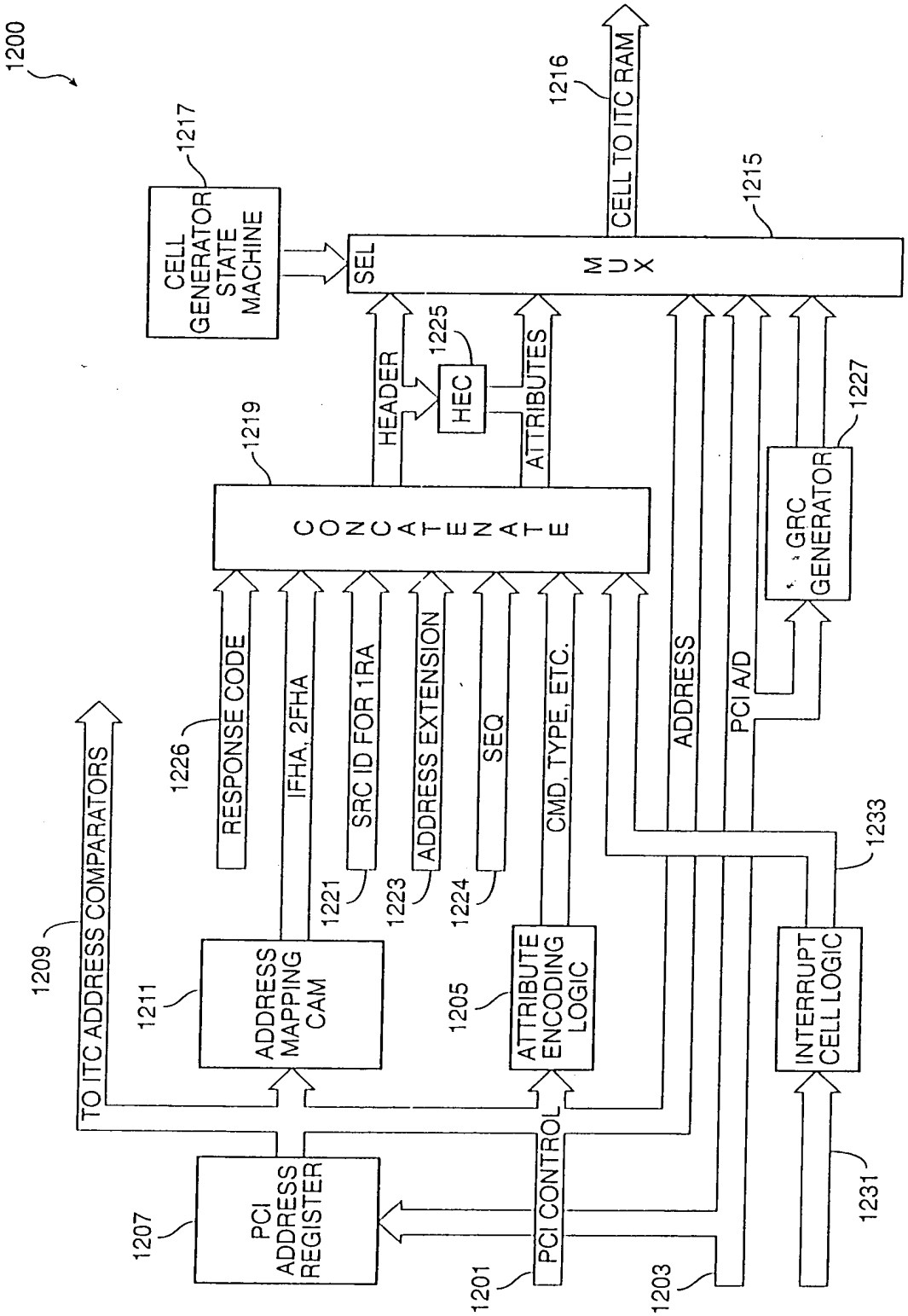
1200
1216
CELL TO ITC RAM
1217
CELL GENERATOR STATE MACHINE
1215
SEL
MUX
HEADER
1225
HEC
ATTRIBUTES
1227
GRC GENERATOR
1219
CONCATENATE
RESPONSE CODE
1226
IFHA, 2FHA
SRC ID FOR 1RA
ADDRESS EXTENSION
SEQ
CMD, TYPE, ETC.
ADDRESS
PCI A/D
1233
TO ITC ADDRESS COMPARATORS
1209
1221
1223
1224
1211
ADDRESS MAPPING CAM
1205
ATTRIBUTE ENCODING LOGIC
INTERRUPT CELL LOGIC
PCI CONTROL
1207
PCI ADDRESS REGISTER
1231
1201
1203

FIG. 12a

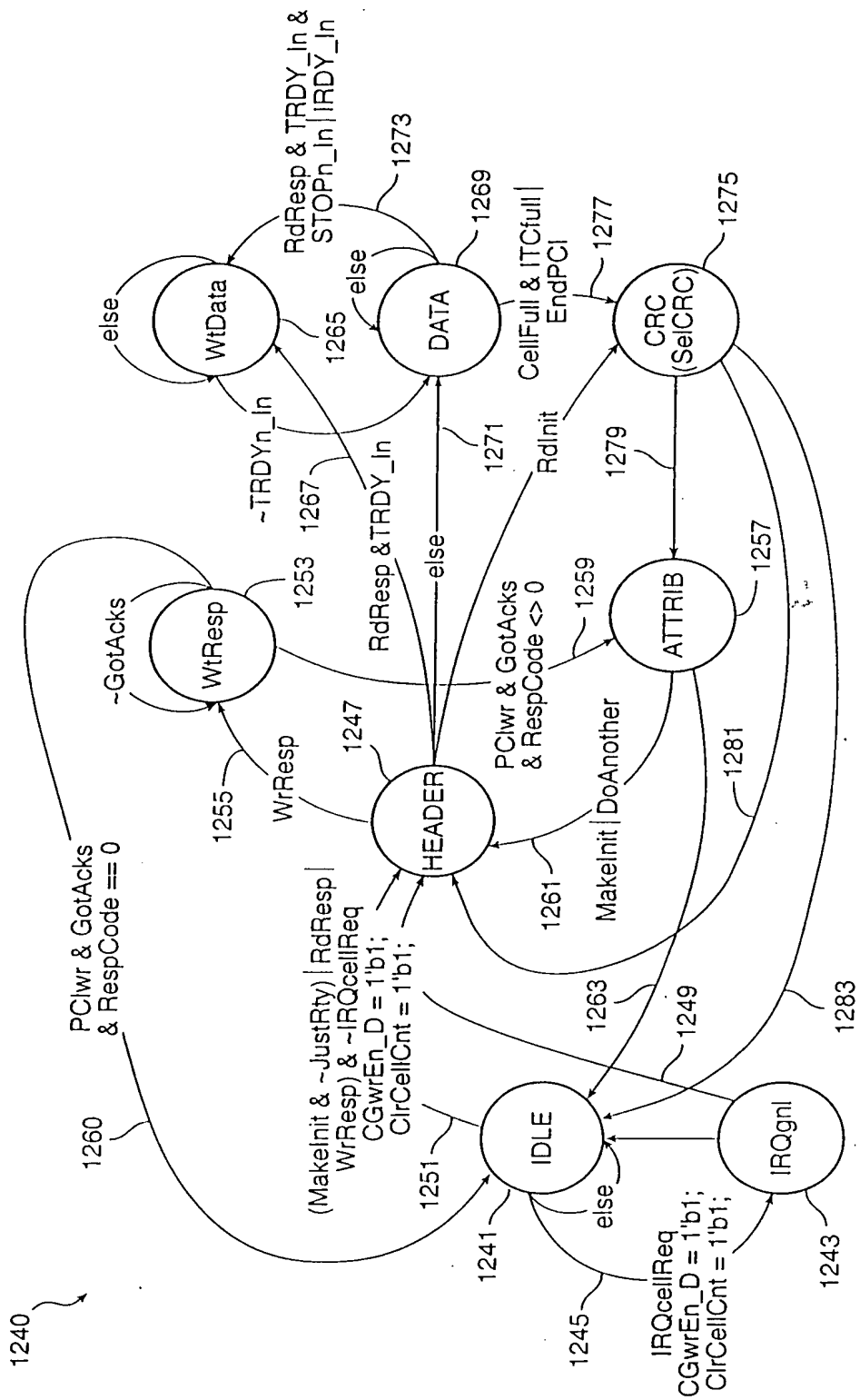
1240
IDLE
1251
WtResp
1253
HEADER
1247
WtData
1265
DATA
1269
ATTRIB
1257
CRC (SelCRC)
1275
IRQgnl
1243
1260
PCIwr & GotAcks & RespCode == 0
(MakeInit & ~JustRty) | RdResp | WrResp) & ~IRQcellReq
CGwrEn_D = 1'b1;
ClrCellCnt = 1'b1;
1241
else
1245
IRQcellReq
CGwrEn_D = 1'b1;
ClrCellCnt = 1'b1;
1263
1249
1283
1255
WrResp
~GotAcks
else
1261
MakeInit | DoAnother
PCIwr & GotAcks & RespCode <> 0
1259
RdResp &TRDY_In
else
1271
1267
~TRDYn_In
RdResp & TRDY_In & STOPn_In | IRDY_In
1273
else
1279
RdInit
CellFull & ITCfull | EndPCI
1277
1281

FIG. 12b

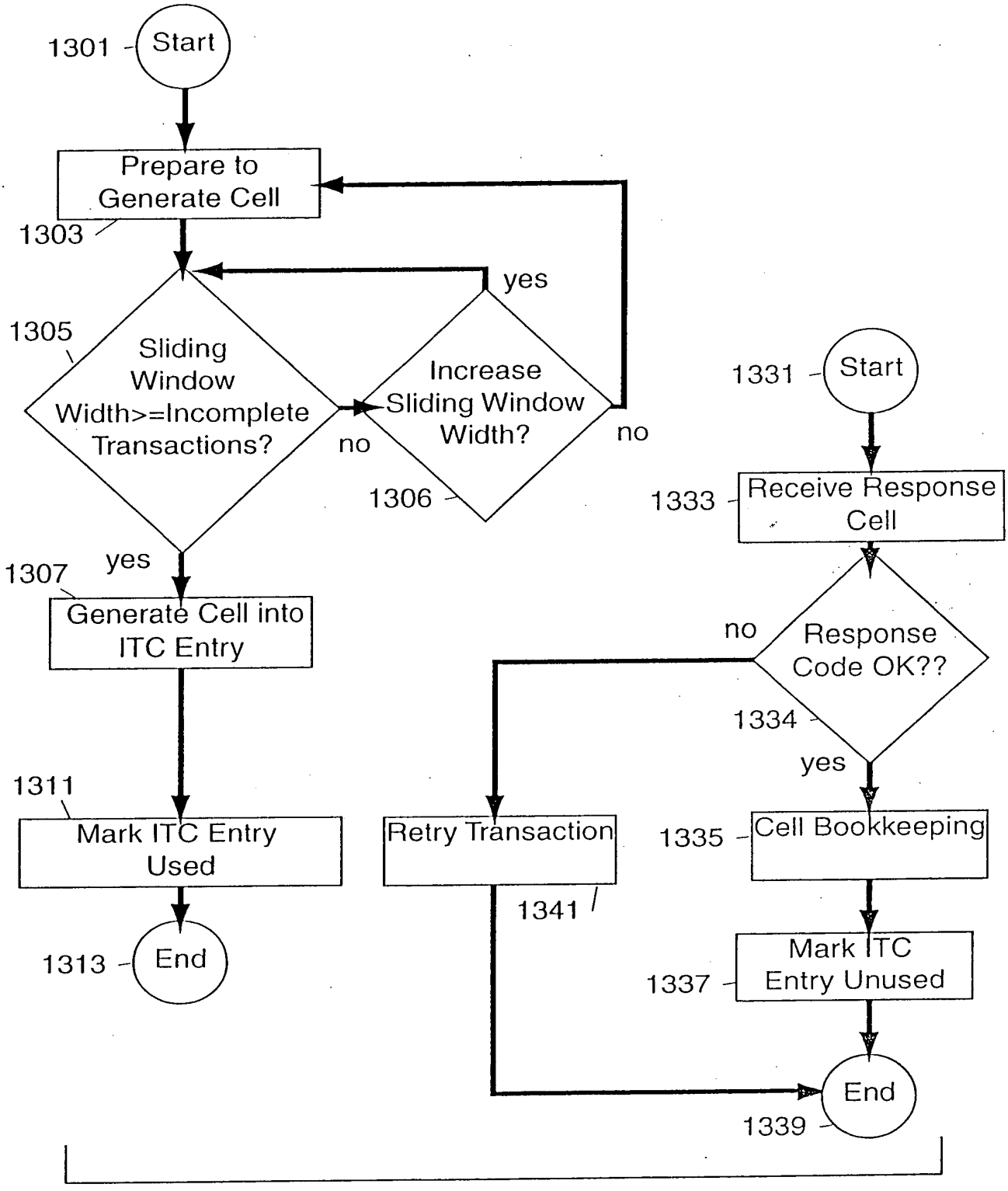
1301
Start
Prepare to Generate Cell
1303
1305
Sliding Window Width>=Incomplete Transactions?
yes
no
Increase Sliding Window Width?
yes
no
1306
1307
yes
Generate Cell into ITC Entry
1311
Mark ITC Entry Used
1313
End
1331
Start
1333
Receive Response Cell
no
Response Code OK??
1334
yes
Retry Transaction
1341
1335
Cell Bookkeeping
Mark ITC Entry Unused
1337
End
1339

Fig. 13a

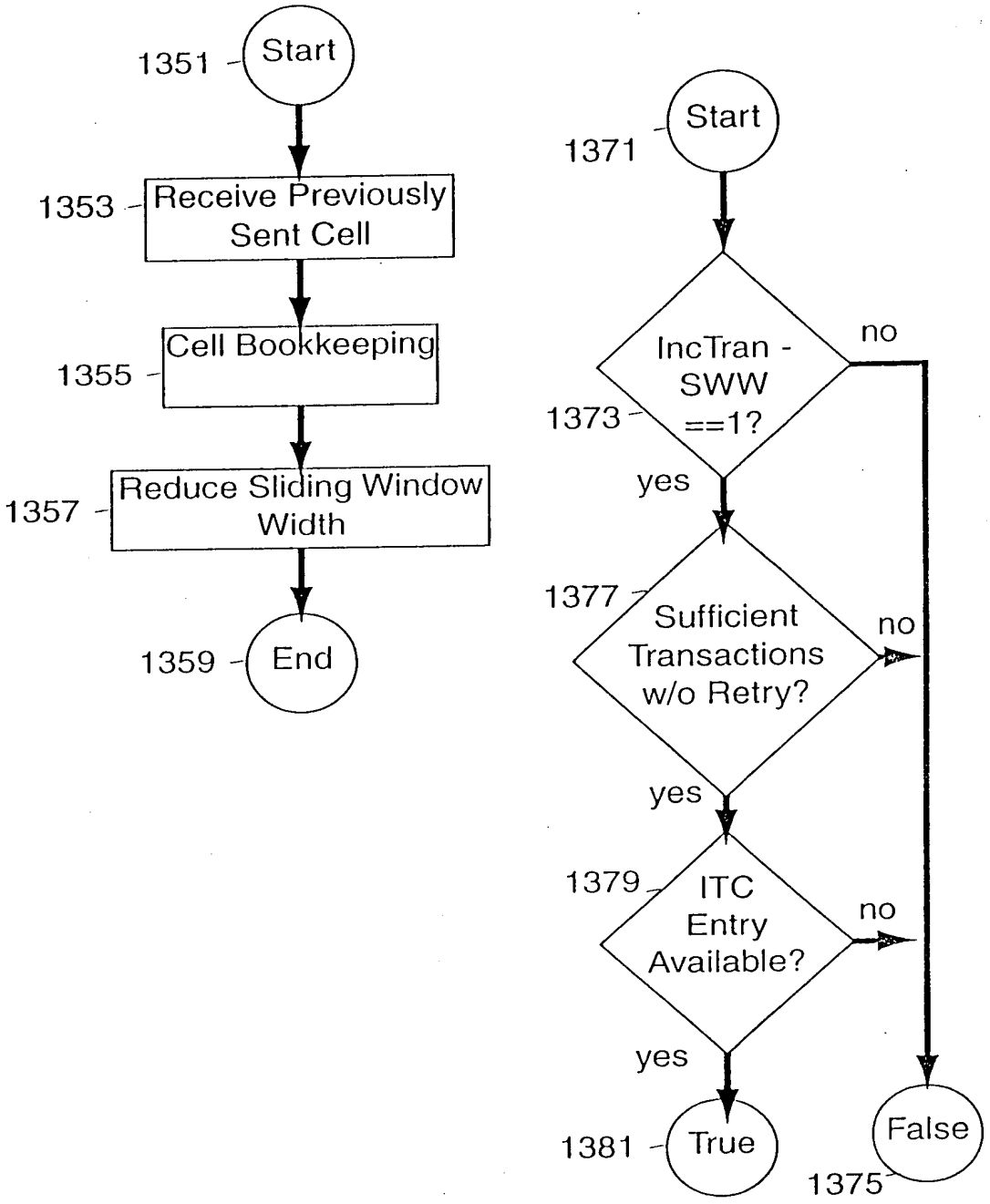
1351
Start
1353
Receive Previously Sent Cell
1355
Cell Bookkeeping
1357
Reduce Sliding Window Width
1359
End
1371
Start
IncTran - SWW ==1?
1373
no
yes
1377
Sufficient Transactions w/o Retry?
no
yes
1379
ITC Entry Available?
no
yes
1381
True
False
1375

Fig. 13b

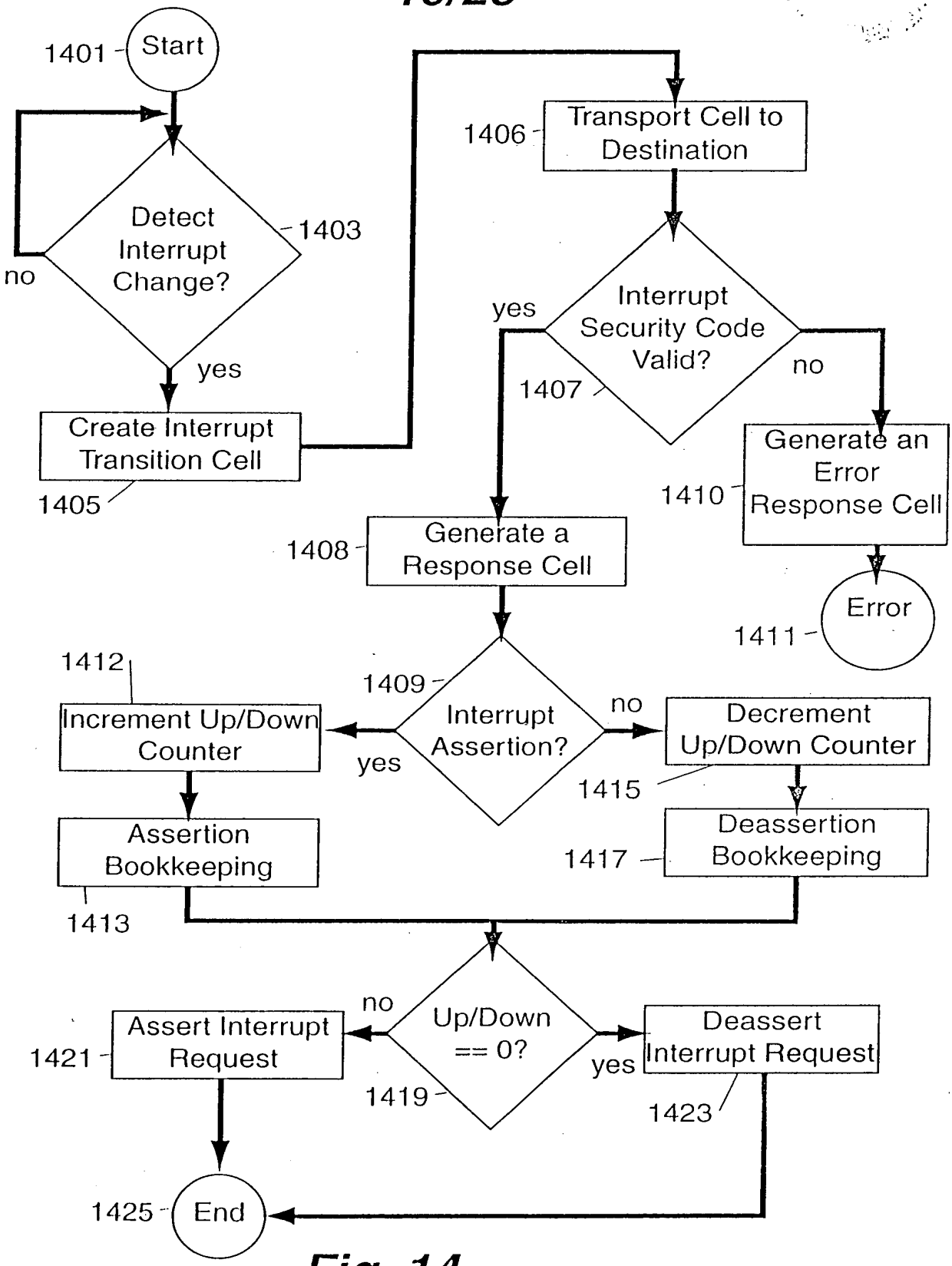
1401
Start
Detect Interrupt Change?
1403
no
yes
Create Interrupt Transition Cell
1405
1406
Transport Cell to Destination
Interrupt Security Code Valid?
1407
yes
no
Generate an Error Response Cell
1410
Error
1411
1408
Generate a Response Cell
1409
Interrupt Assertion?
yes
no
1412
Increment Up/Down Counter
Decrement Up/Down Counter
1415
Assertion Bookkeeping
1413
Deassertion Bookkeeping
1417
Up/Down == 0?
no
yes
1419
1421
Assert Interrupt Request
Deassert Interrupt Request
1423
1425
End

Fig. 14

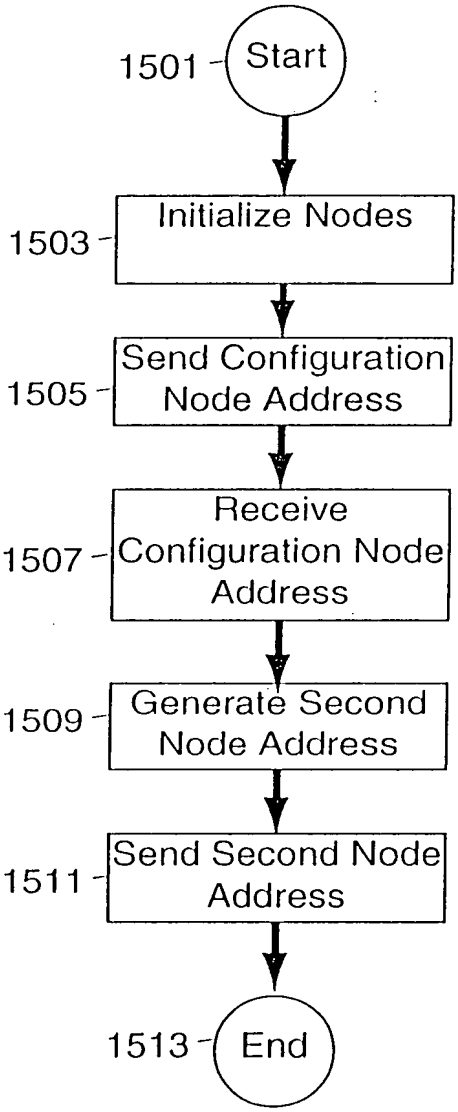
1501
Start
1503
Initialize Nodes
1505
Send Configuration Node Address
1507
Receive Configuration Node Address
1509
Generate Second Node Address
1511
Send Second Node Address
1513
End

Fig. 15

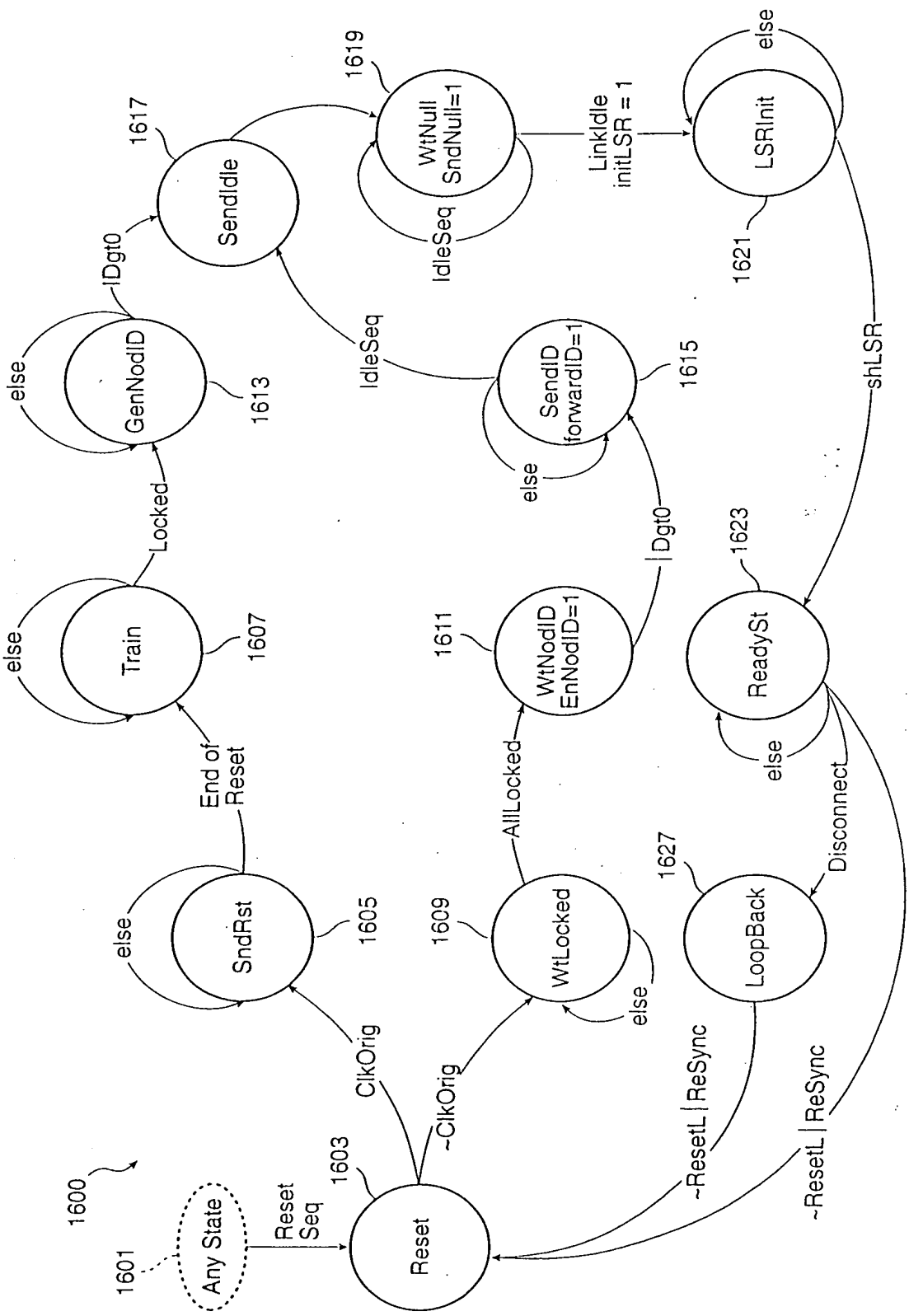
1600
1601
Any State
Reset Seq
1603
Reset
~ClkOrig
ClkOrig
1605
SndRst
else
End of Reset
1607
Train
else
Locked
1613
GenNodID
else
IDgt0
1617
SendIdle
1619
WtNull
SndNull=1
IdleSeq
LinkIdle
initLSR = 1
1621
LSRInit
else
shLSR
1623
ReadySt
else
Disconnect
~ResetL | ReSync
1627
LoopBack
~ResetL | ReSync
1609
WtLocked
else
AllLocked
1611
WtNodID
EnNodID=1
Dgt0
1615
SendID
forwardID=1
else
IdleSeq

FIG. 16

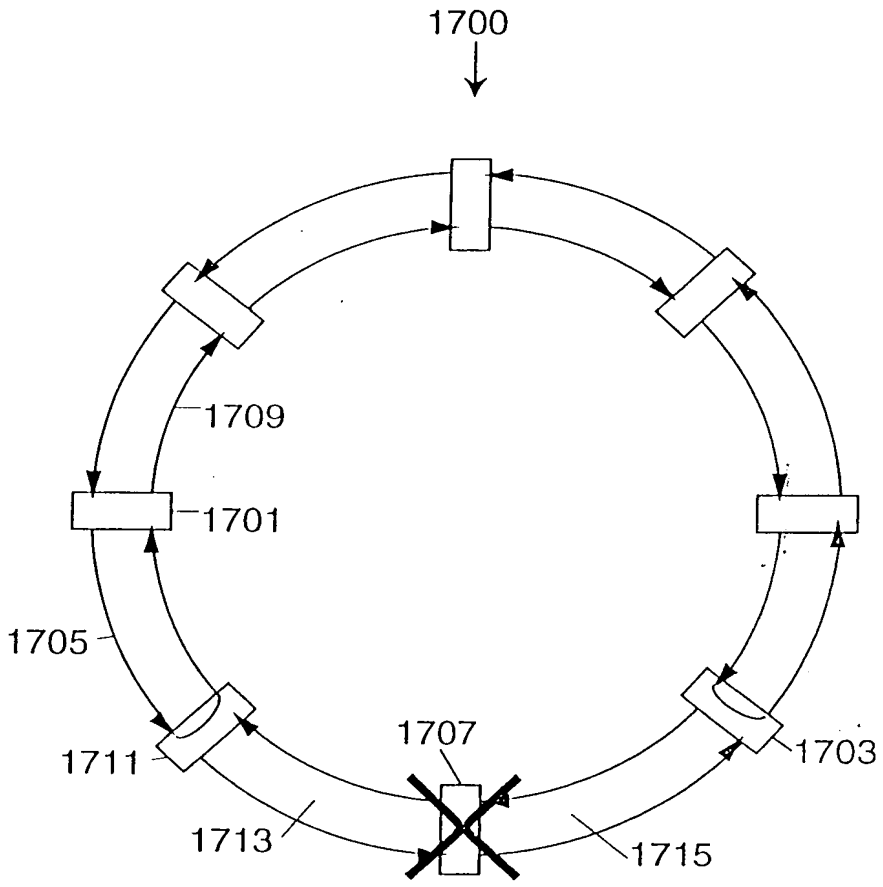

Fig. 17

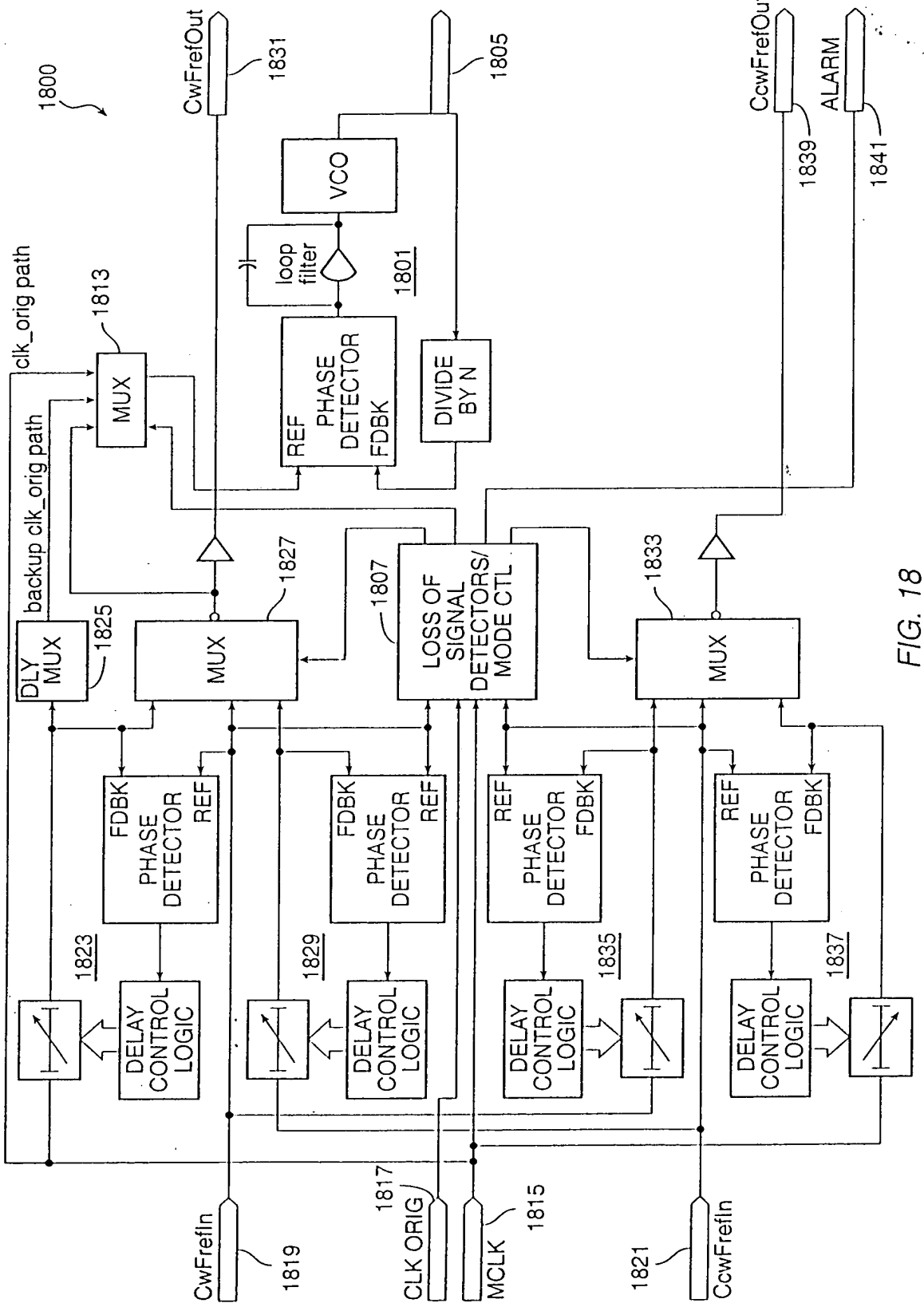
1800
CwFrefOut
1831
1805
CcwFrefOut
1839
ALARM
1841
VCO
loop filter
1801
clk_orig path
1813
MUX
REF
PHASE DETECTOR
FDBK
DIVIDE BY N
backup clk_orig path
DLY MUX
1825
MUX
1827
1807
LOSS OF SIGNAL DETECTORS/ MODE CTL
1833
MUX
FDBK
PHASE DETECTOR
REF
1823
DELAY CONTROL LOGIC
1829
1835
1837
1817
CLK ORIG
MCLK
1815
CwFrefIn
1819
1821
CcwFrefIn

FIG. 18

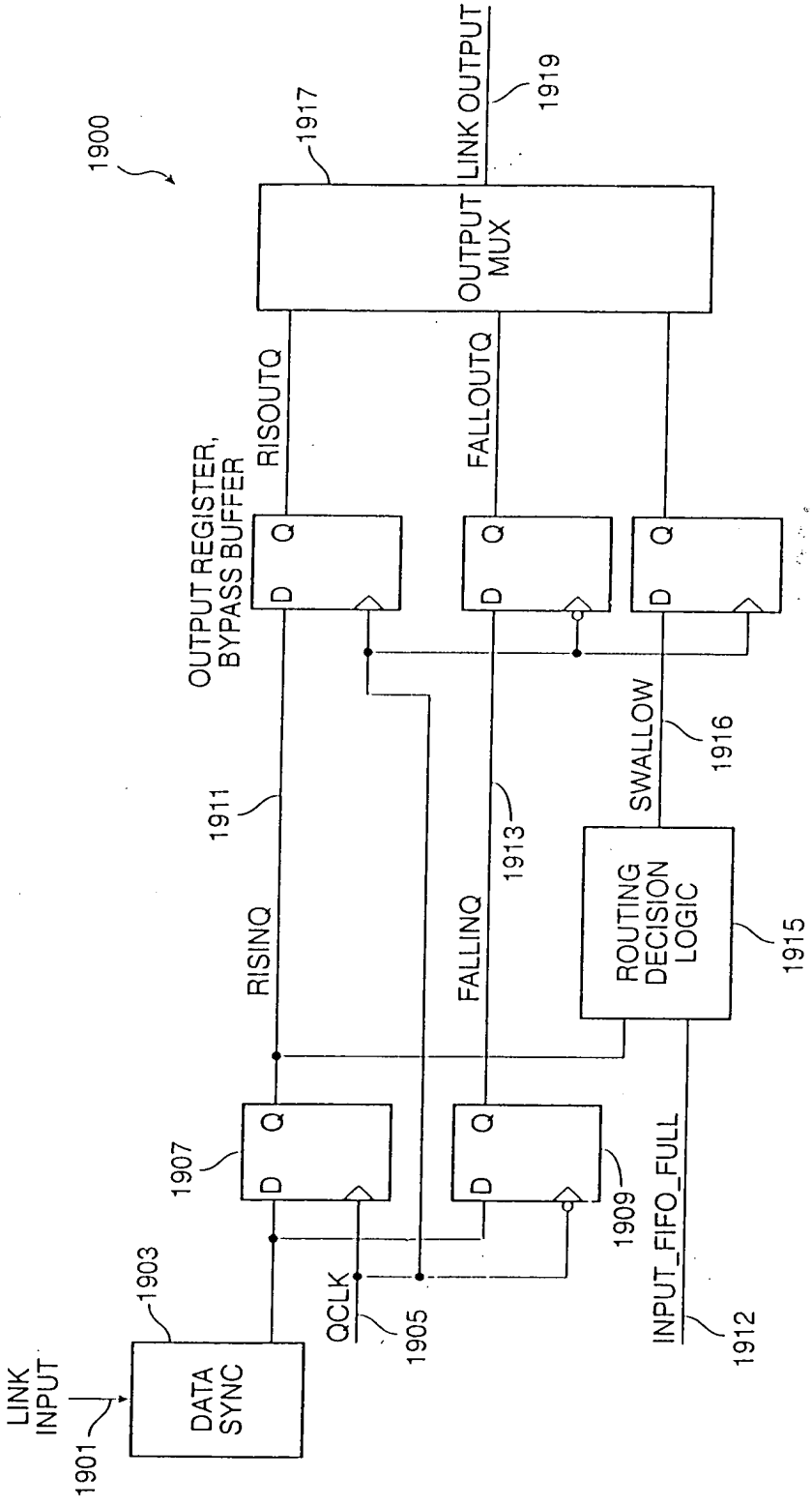
1900
1917
LINK OUTPUT
1919
OUTPUT MUX
RISOUTQ
FALLOUTQ
OUTPUT REGISTER, BYPASS BUFFER
Q
D
1911
1913
SWALLOW
1916
RISINQ
FALLINQ
ROUTING DECISION LOGIC
1915
1907
1909
INPUT_FIFO_FULL
1912
1903
QCLK
1905
LINK INPUT
1901
DATA SYNC

FIG. 19a

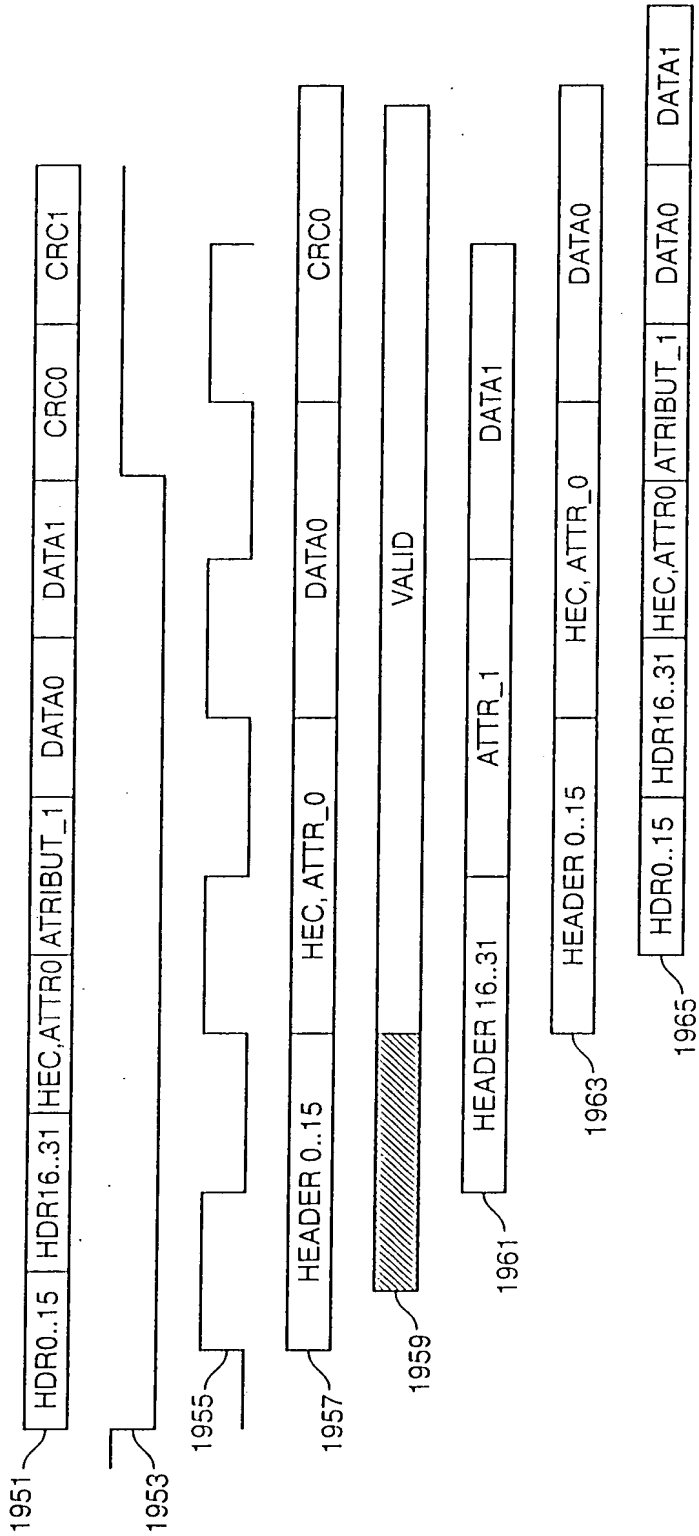
HDR0..15
HDR16..31
HEC,ATTR0
ATRIBUT_1
DATA0
DATA1
CRC0
CRC1
1951
1953
1955
HEADER 0..15
HEC, ATTR_0
DATA0
CRC0
1957
1959
VALID
HEADER 16..31
ATTR_1
DATA1
1961
HEADER 0..15
HEC, ATTR_0
DATA0
1963
HDR0..15
HDR16..31
HEC,ATTR0
ATRIBUT_1
DATA0
DATA1
1965

FIG. 19b

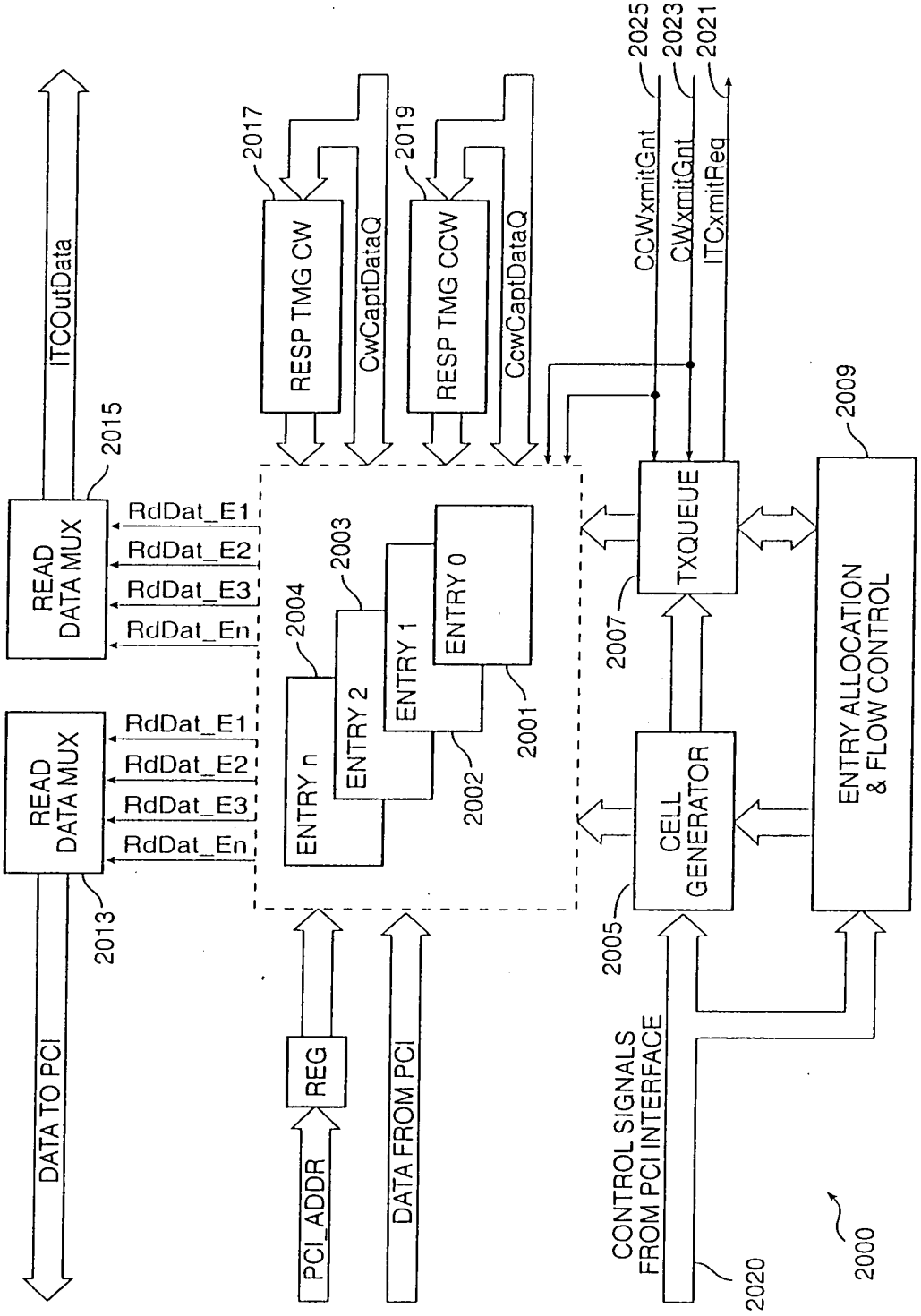
ITCOutData
2015
READ DATA MUX
RdDat_E1
RdDat_E2
RdDat_E3
RdDat_En
READ DATA MUX
RdDat_E1
RdDat_E2
RdDat_E3
RdDat_En
2013
DATA TO PCI
2017
RESP TMG CW
CwCaptDataQ
2019
RESP TMG CCW
CcwCaptDataQ
2003
2004
ENTRY n
ENTRY 2
ENTRY 1
ENTRY 0
2001
2002
REG
PCI_ADDR
DATA FROM PCI
2025
2023
2021
CCWxmitGnt
CWxmitGnt
ITCxmitReq
2009
TXQUEUE
2007
ENTRY ALLOCATION & FLOW CONTROL
CELL GENERATOR
2005
CONTROL SIGNALS FROM PCI INTERFACE
2020
2000

FIG. 20

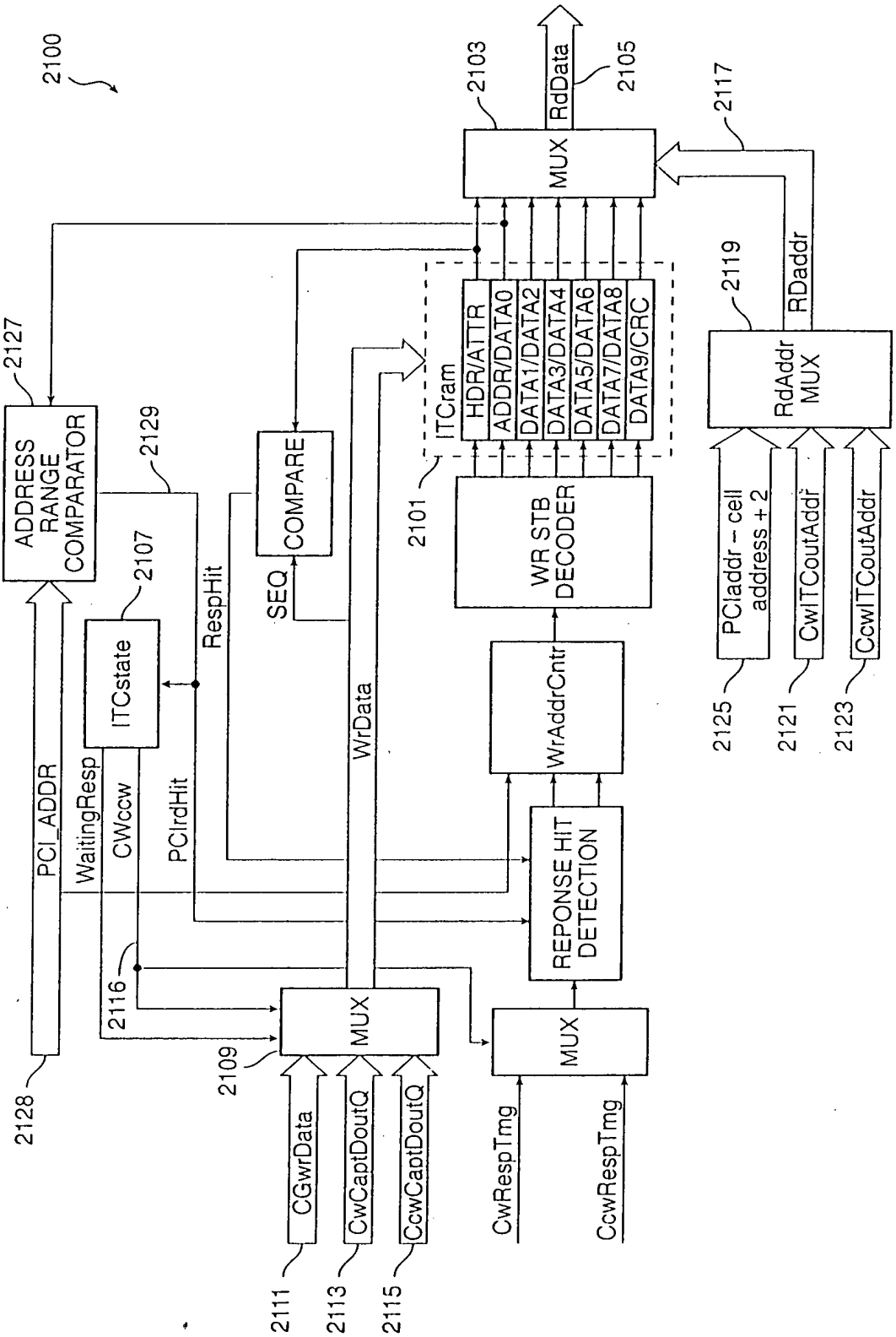
2100
2103
RdData
2105
2117
MUX
2127
ADDRESS RANGE COMPARATOR
2129
COMPARE
ITCram
HDR/ATTR
ADDR/DATA0
DATA1/DATA2
DATA3/DATA4
DATA5/DATA6
DATA7/DATA8
DATA9/CRC
2119
RDaddr
RdAddr MUX
2101
WR STB DECODER
2107
ITCstate
RespHit
SEQ
WrData
WrAddrCntr
PCI_ADDR
WaitingResp
CWccw
PCIrdHit
REPONSE HIT DETECTION
PCladdr – cell address + 2
CwITCoutAddr
CcwITCoutAddr
2125
2121
2123
2116
2109
MUX
MUX
2128
CGwrData
CwCaptDoutQ
CcwCaptDoutQ
CwRespTmg
CcwRespTmg
2111
2113
2115

FIG. 21

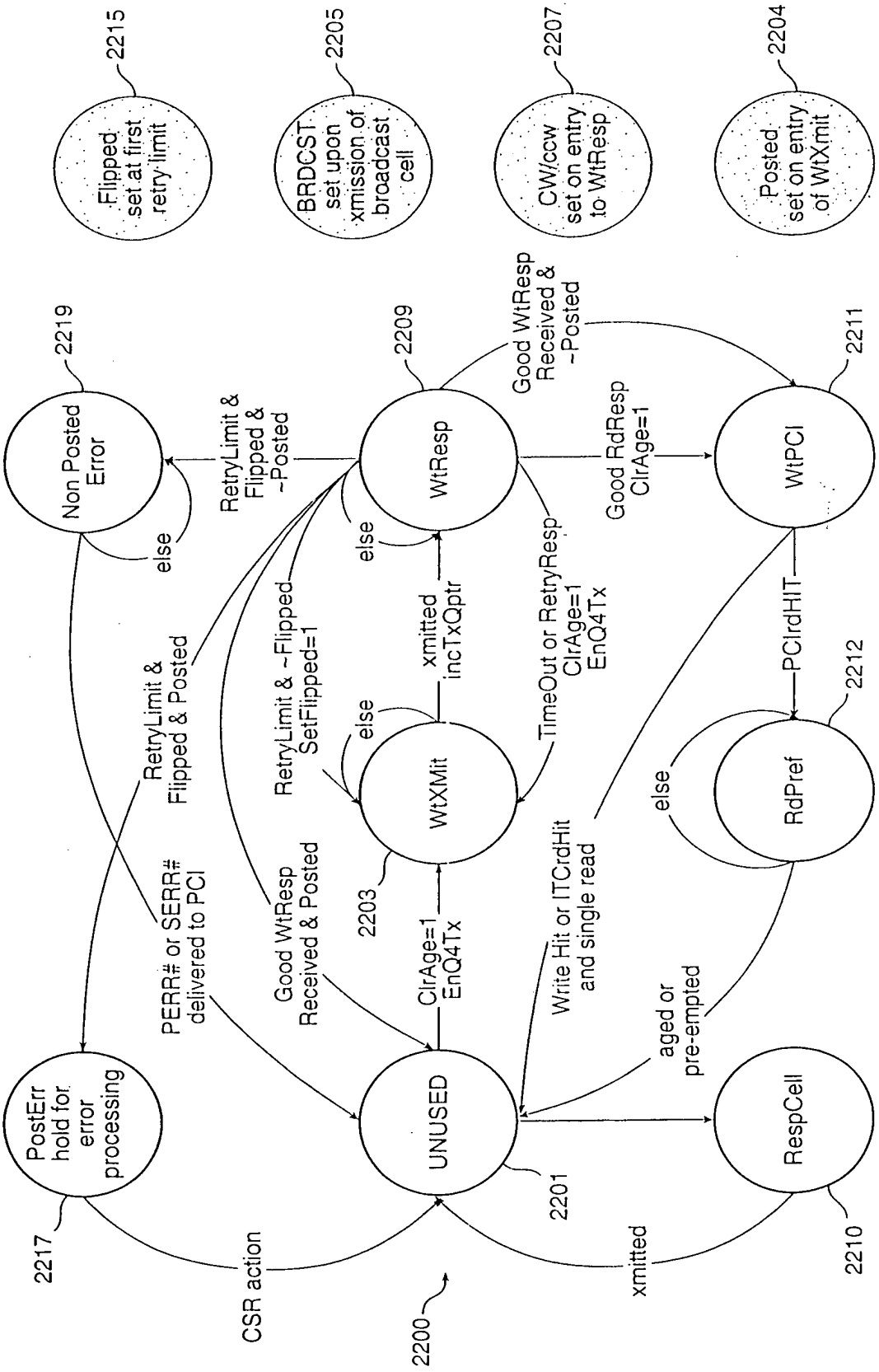
2215
Flipped
set at first
retry limit
2205
BRDCST
set upon
xmission of
broadcast
cell
2207
CW/ccw
set on entry
to WtResp
2204
Posted
set on entry
of WtXmit
2219
Non Posted
Error
2209
WtResp
2211
WtPCI
2203
WtXMit
2212
RdPref
2201
UNUSED
2217
PostErr
hold for
error
processing
2210
RespCell
2200
RetryLimit &
Flipped & Posted
else
RetryLimit &
Flipped &
~Posted
else
Good WtResp
Received &
~Posted
Good RdResp
ClrAge=1
RetryLimit & ~Flipped
SetFlipped=1
else
xmitted
incTxQptr
TimeOut or RetryResp
ClrAge=1
EnQ4Tx
PCIrdHIT
else
PERR# or SERR#
delivered to PCI
Good WtResp
Received & Posted
ClrAge=1
EnQ4Tx
Write Hit or ITCrdHit
and single read
aged or
pre-empted
CSR action
xmitted

FIG. 22